

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND1
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : SGND2
 LAYER 8 : BOT

- CPU CORE SC452 PAG 38
- VGACORE(1.025V)MAX1993 PAG 39
- INT-VGACORE MAX8776 PAG 40
- VCCP +1.5V AND GMCH 1.05V(TPS51124) PAG 41
- SYSTEM POWER MAX8734 PAG 42
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116) PAG 43
- SYSTEM CHARGER(MAX8724) PAG 45,46

Voltage Rails

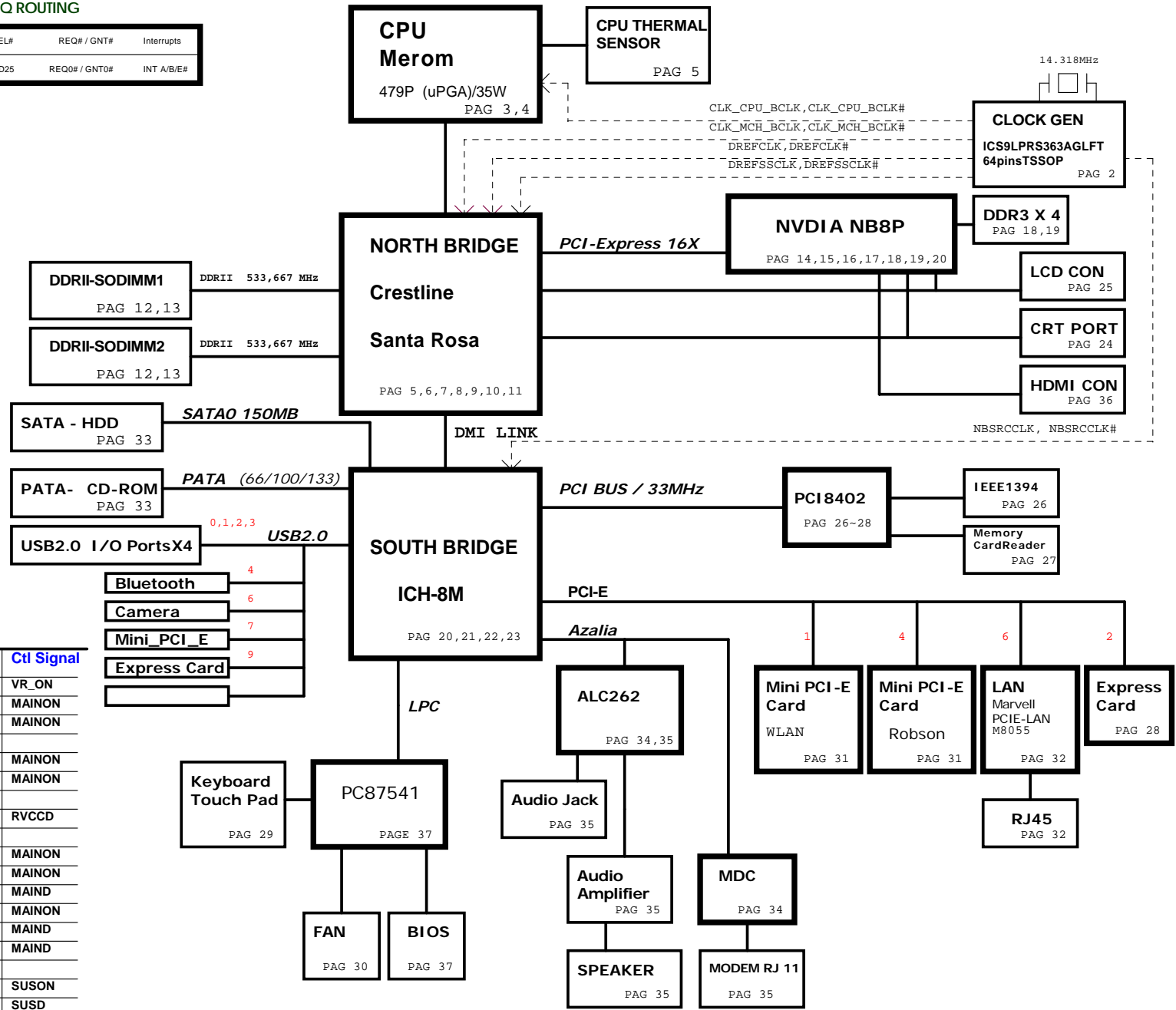
| Voltage Rails | ON S0-S2 | ON S3 | ON S4 | ON S5 | Ctl Signal |
|---------------|----------|-------|-------|-------|------------|
| VCC_CORE | X | | | | VR_ON |
| VCCP | X | | | | MAINON |
| SMDDR_VTERM | X | | | | MAINON |
| VGACORE | X | | | | MAINON |
| VGA1.2 | X | | | | MAINON |
| RVCC3 | X | X | X | | RVCCD |
| VCC1.25 | X | | | | MAINON |
| VCC1.5 | X | | | | MAINON |
| VCC1.8 | X | | | | MAIND |
| VCC2.5 | X | | | | MAINON |
| VCC3 | X | | | | MAIND |
| VCC5 | X | | | | MAIND |
| 1.8VSUS | X | X | | | SUSON |
| 3VSUS | X | X | | | SUSD |
| 5VSUS | X | X | | | SUSD |
| 3VPCU | X | X | X | X | 8734LDO5 |
| 5VPCU | X | X | X | X | 8734LDO5 |
| 15VPCU | X | X | X | X | 5VPCU |

CH3 BLOCK DIAGRAM

01

PCI DEVICES IRQ ROUTING

| PCI DEVICE | IDSEL# | REQ# / GNT# | Interrupts |
|------------|--------|---------------|------------|
| PCI8402 | AD25 | REQ0# / GNT0# | INT A/B/E# |

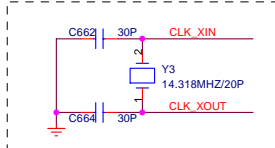
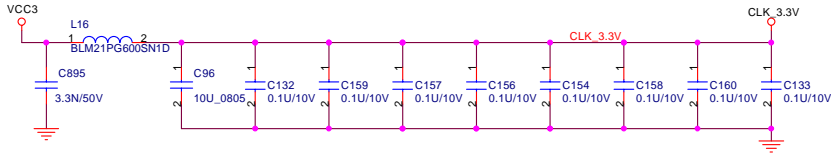


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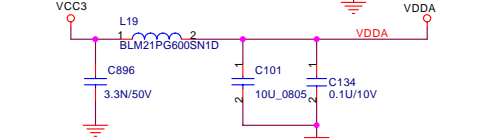
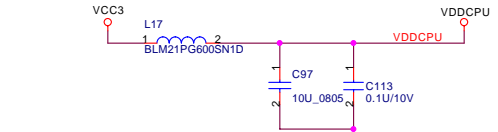
| | | |
|--|-----------------|-----|
| Size | Document Number | Rev |
| BLOCK DIAGRAM | 1A | 1A |
| Date: Tuesday, February 06, 2007 Sheet 1 of 46 | | |

hexaimf@hotmail.com

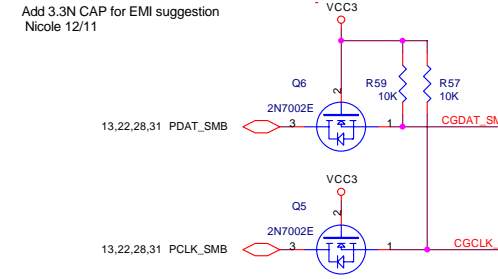
14.318MHz



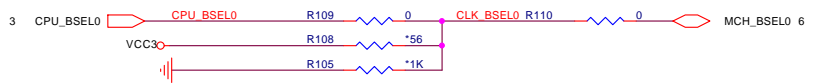
Add 3.3N CAP for EMI suggestion
Nicole 12/11



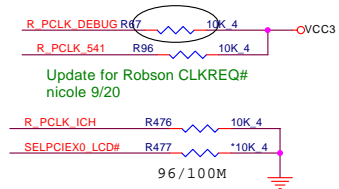
Add 3.3N CAP for EMI suggestion
Nicole 12/11



CPU Clock select



| FSC BSEL2 | FSB BSEL1 | FSA BSEL0 | CPU | SRC | PCI | REF | USB | DOT | Spread % |
|-----------|-----------|-----------|---------------|-----|-------|--------|-----|-----|----------|
| 0 | 0 | 0 | 266.66 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 0 | 0 | 1 | 133.33 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| * 0 | 1 | 0 | 200.00 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 0 | 1 | 1 | 166.66 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 1 | 0 | 0 | 333.33 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 1 | 0 | 1 | 100.00 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 1 | 1 | 0 | 400.00 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |
| 1 | 1 | 1 | 200.00 | 100 | 33.33 | 14.318 | 48 | 96 | 0.5 Down |

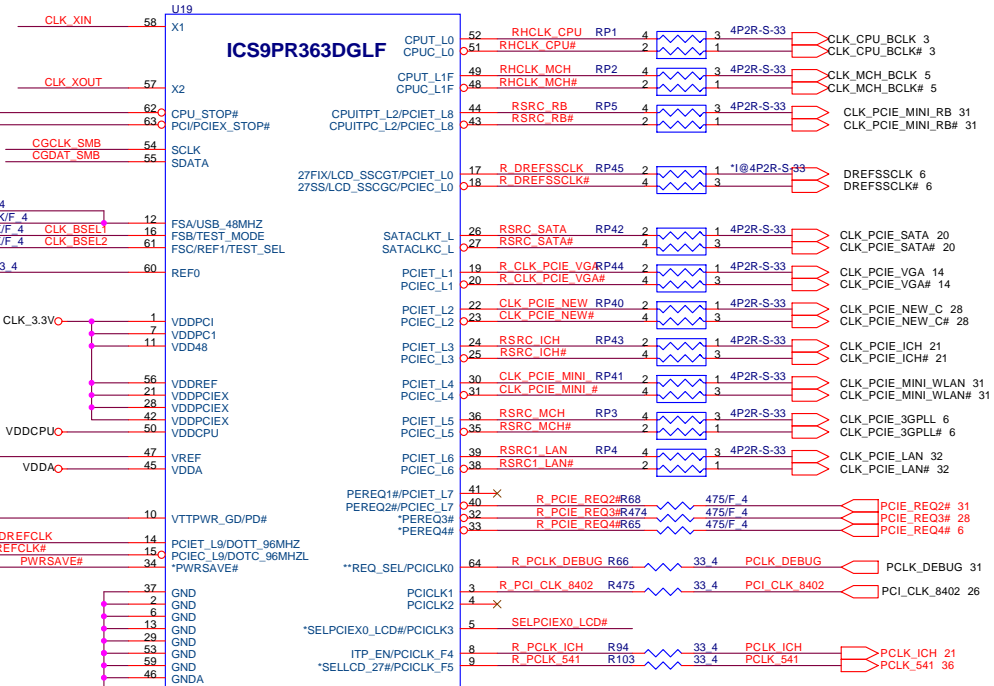


Update for Robson CLKREQ#
nicole 9/20

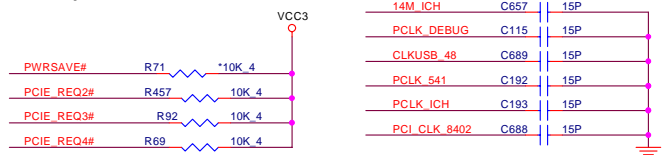
| | |
|-------------|---------------|
| Pin64 | Pin8 |
| 0 PCIEEXCLK | * 0 SRC Pair |
| * 1 PEREQ# | 1 CPUTIP Pair |

| | | | |
|------------|---------|---------|---------|
| PCIE_REQ1# | PCIE_L0 | PCIE_L6 | |
| PCIE_REQ2# | PCIE_L1 | PCIE_L8 | |
| PCIE_REQ3# | PCIE_L2 | PCIE_L4 | |
| PCIE_REQ4# | PCIE_L3 | PCIE_L5 | PCIE_L7 |

internal build-in 33ohm damping resistor
PN change from B version to D version
nicole 12/01



* Internal pull up to VDD
** Internal pull down to GND

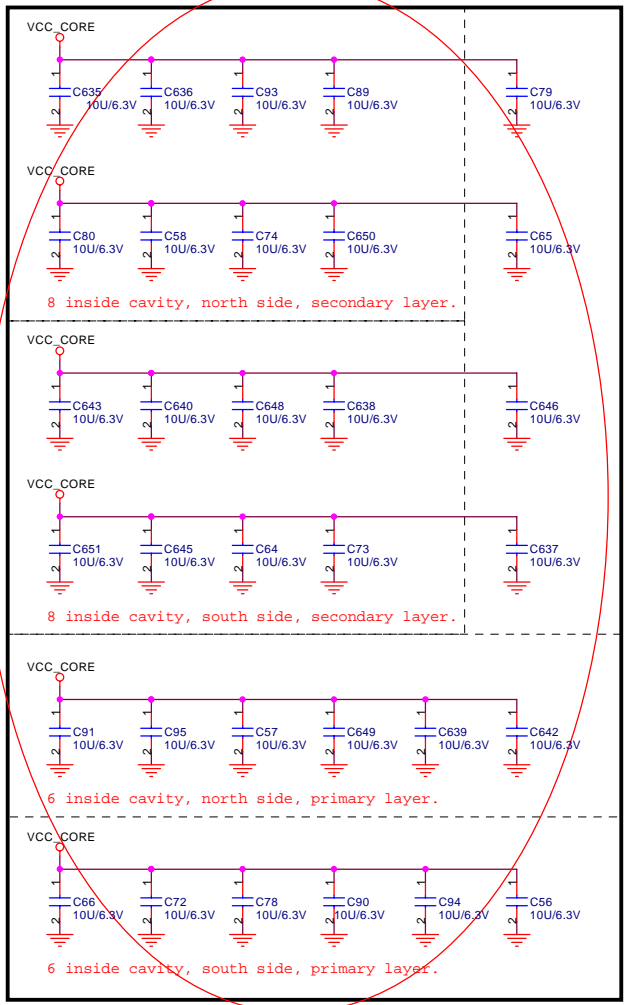


LATCH SELECT TABLE

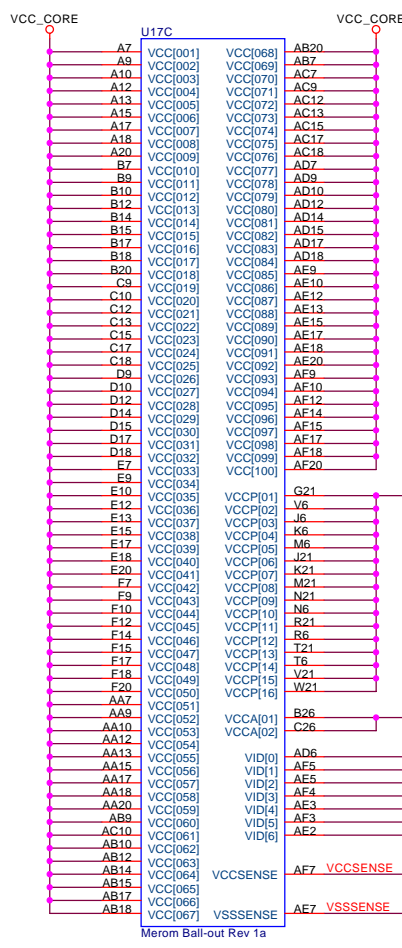
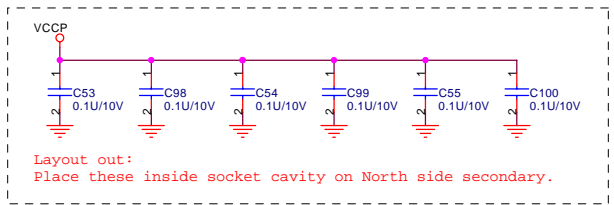
| Pin5 | Pin9 | Pin14/15 | Pin17/18 |
|------|------|----------|----------|
| 0 | 0 | PCIEEX9 | 27MHz |
| 0 | 1 | PCIEEX9 | LCD |
| * 1 | x | DOT96 | PCIEEX0 |

| | |
|-------|------------------|
| REQ2# | used for ROBSON |
| REQ3# | used for NEWCARD |
| REQ4# | used for GMCH |

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



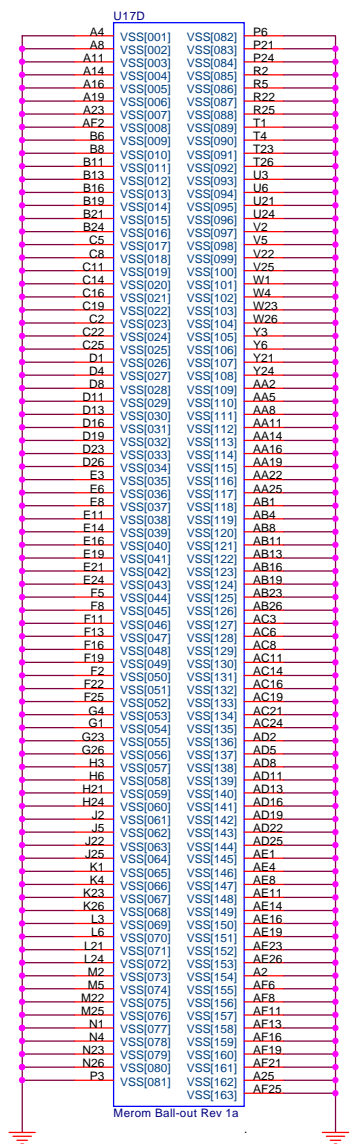
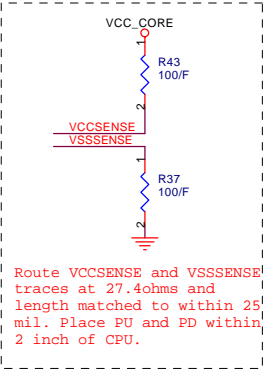
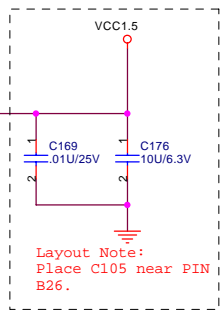
Update to 10u *32pcs. OK

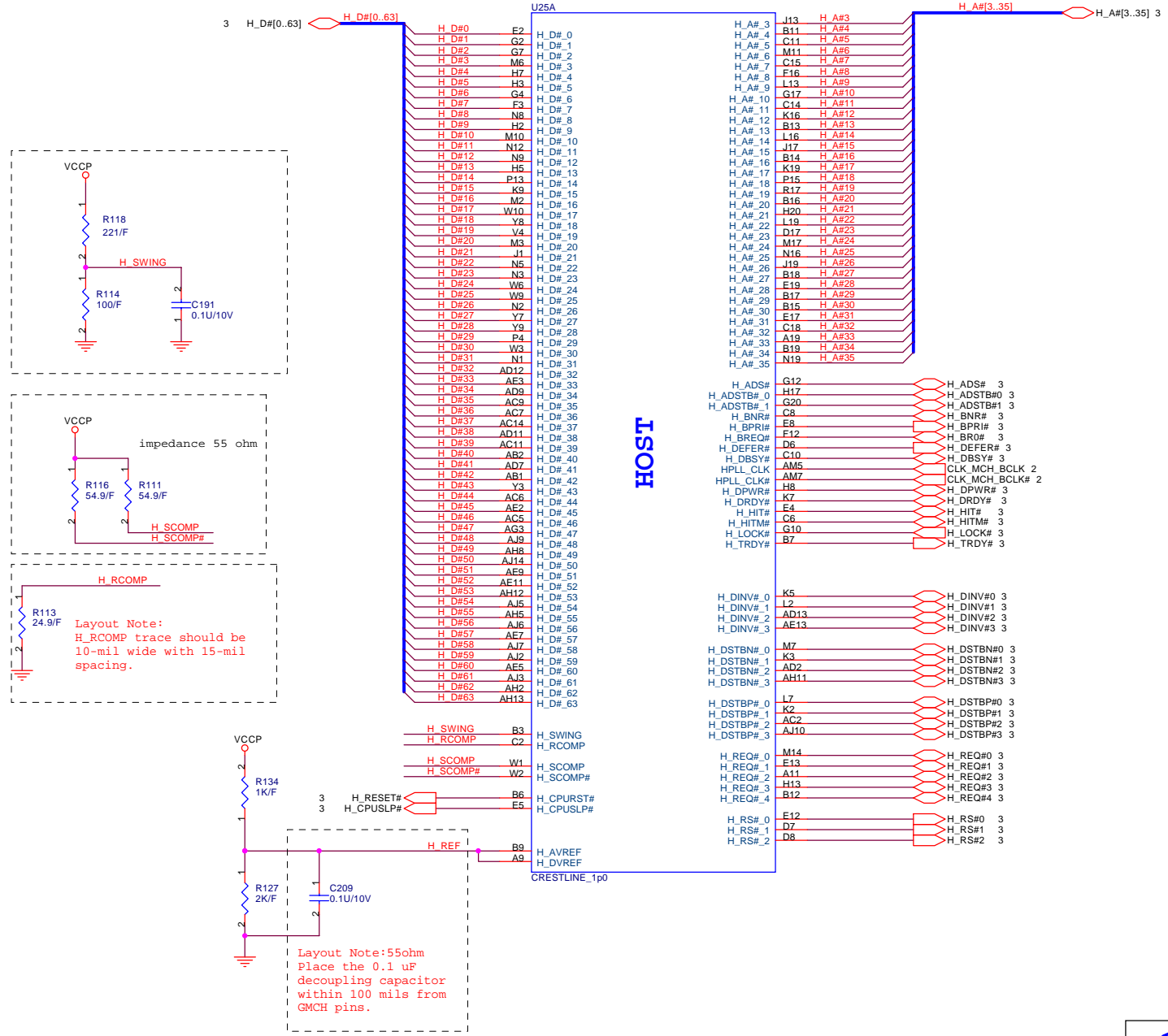


ICCODE:
for Merom processors
recommended design
target is 44A

ICCP:
before vccore stable
peak current is 4.5A
2. after vccore stable
continue current is
2.5A

ICCA 130mA





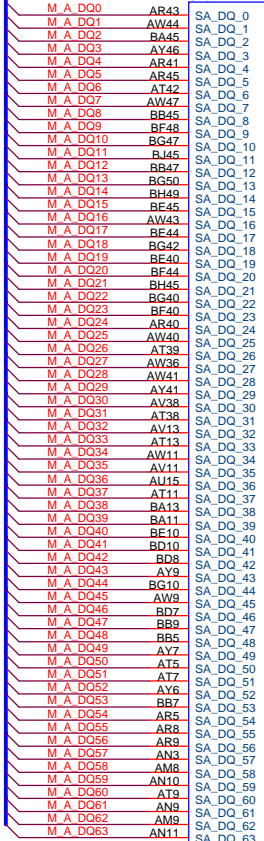
Layout Note:
 H_RCOMP trace should be
 10-mil wide with 15-mil
 spacing.

Layout Note: 55ohm
 Place the 0.1 uF
 decoupling capacitor
 within 100 mils from
 GMCH pins.

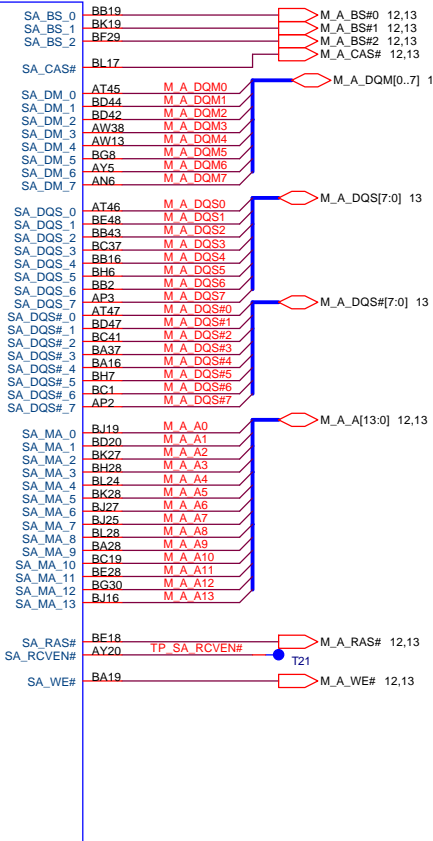
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| Size | Document Number | Rev |
| | NB | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 5 of 46 |

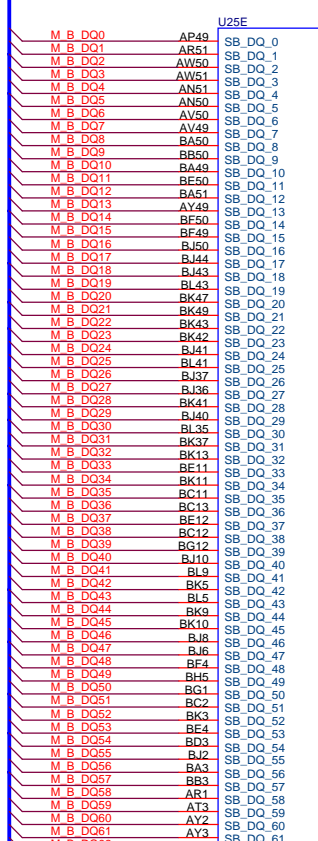
13 M_A_DQ[63:0]



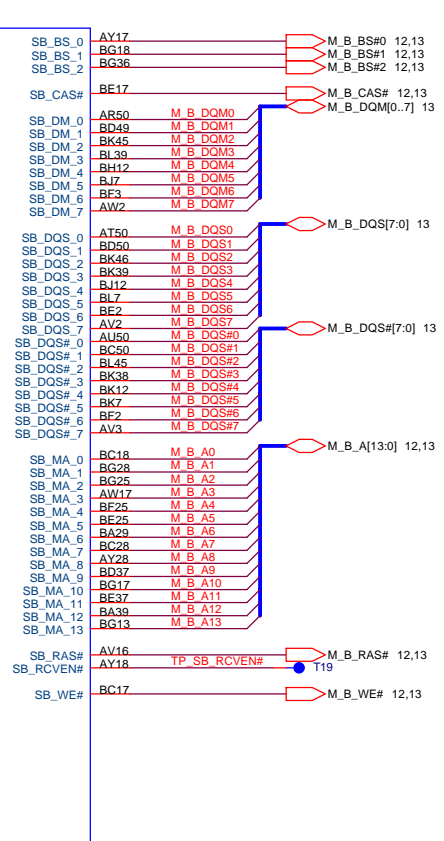
DDR SYSTEM MEMORY A



13 M_B_DQ[63:0]



DDR SYSTEM MEMORY B

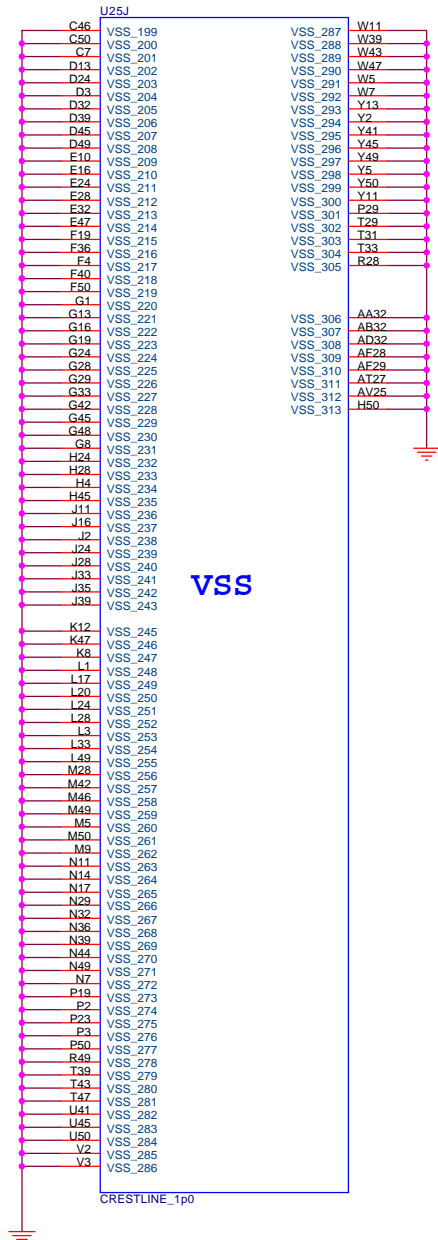
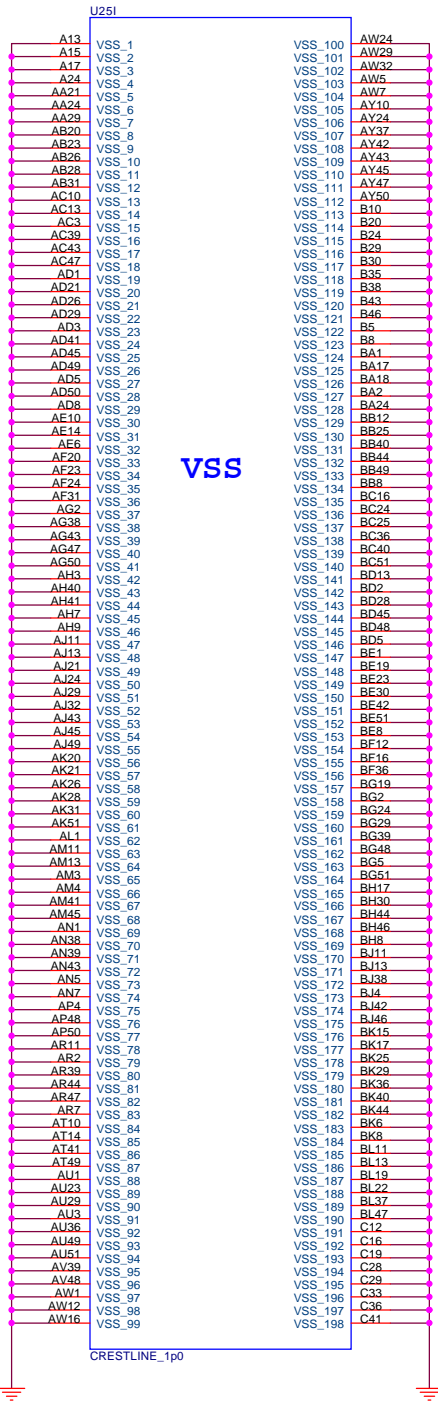


CRESTLINE_1p0

CRESTLINE_1p0

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|-------|----------------------------|---------------|
| Size | Document Number | Rev |
| | NB | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 7 of 46 |



PROJECT : CH3
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| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | NB | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 10 of 46 |

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up

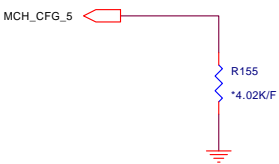
CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

| Pin Name | Strap description | Configuration |
|---------------|------------------------------------|--|
| CFG[2:0] | FSB Frequency Select | 010 = FSB 800MHz 011 = FSB 667MHz |
| CFG[4:3] | Reserved | |
| CFG5 | DMI X2 Select | 0 = DMI X2 1 = DMI X4(Default) |
| CFG6 | Reserved | |
| CFG7 | CPU Strap | 0 = Reserved 1 = Mobile CPU(Default) |
| CFG8 | Low power PCI Express | 0 = Normal mode 1 = Low Power mode |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes 1 = Normal operation(Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ALLZ | 00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default) |
| CFG[18:17] | Reserved | |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card present(Default) 1 = SDVO Card Present |
| CFG19 | DMI Lane Reversal | 0 = Normal operation(Default) 1 = Reverse Lanes |
| CFG20 | SDVO/PCIe concurrent | 0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |

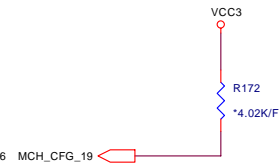
DMI X2 Select

| | |
|-----------|---------------------------------------|
| MCH_CFG_5 | Low = DMIX2 High = IDMIX4(Default) |
|-----------|---------------------------------------|



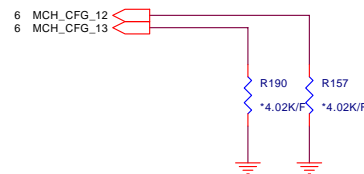
DMI Lane Reversal

| | |
|------------|--|
| MCH_CFG_19 | Low = Normal operation(Default) High = Reverse Lane |
|------------|--|



XOR /ALLZ /Clock Un-gating

| MCH_CFG | 12MCH_CFG_13 | Configuration |
|---------|--------------|---------------------------|
| 0 | 0 | Clock gating disable |
| 0 | 1 | XOR Mode Enable |
| 1 | 0 | ALL-z Mode Enable |
| 1 | 1 | Normal operation(Default) |



PCI Express Graphics

| | |
|-----------|--|
| MCH_CFG_9 | Low = Reverse Lane High = Normal operation(Default) |
|-----------|--|

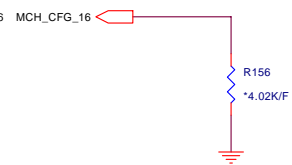


SDVO Present

Strap define at External DVI control page

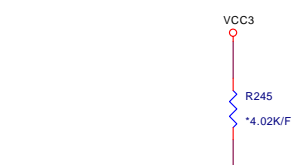
FSB Dynamic ODT

| | |
|------------|---|
| MCH_CFG_16 | Low = ODT Disable High = ODT Enable(Default) |
|------------|---|



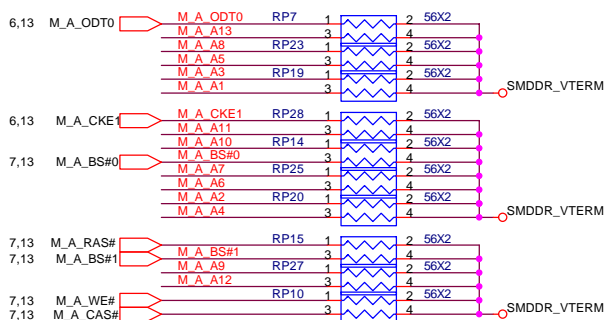
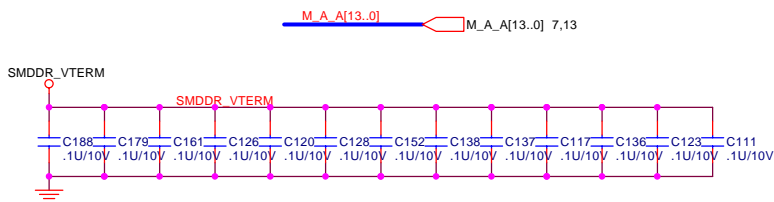
SDVO/PCIe Concurrent operation

| | |
|------------|---|
| MCH_CFG_20 | Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port |
|------------|---|



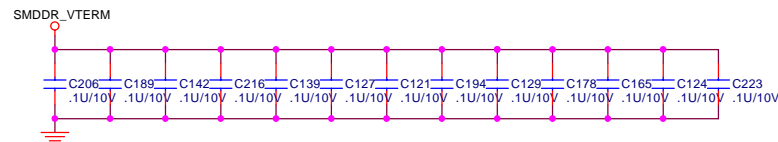
DDRII DUAL CHANNEL A,B

DDRII A CHANNEL

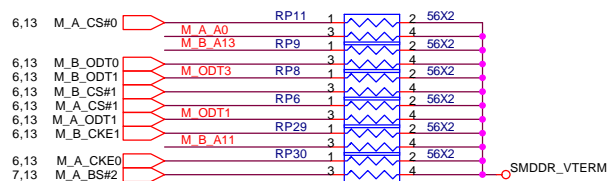
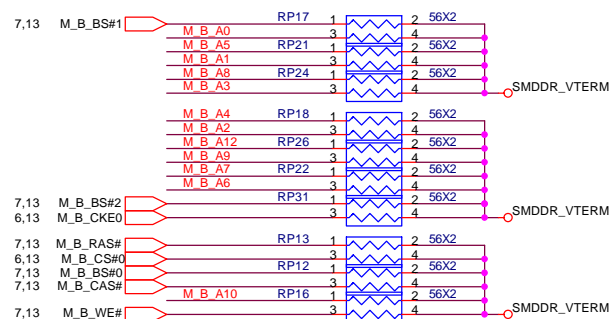


M_B A[13..0] M_B_A[13..0] 7,13

DDRII B CHANNEL

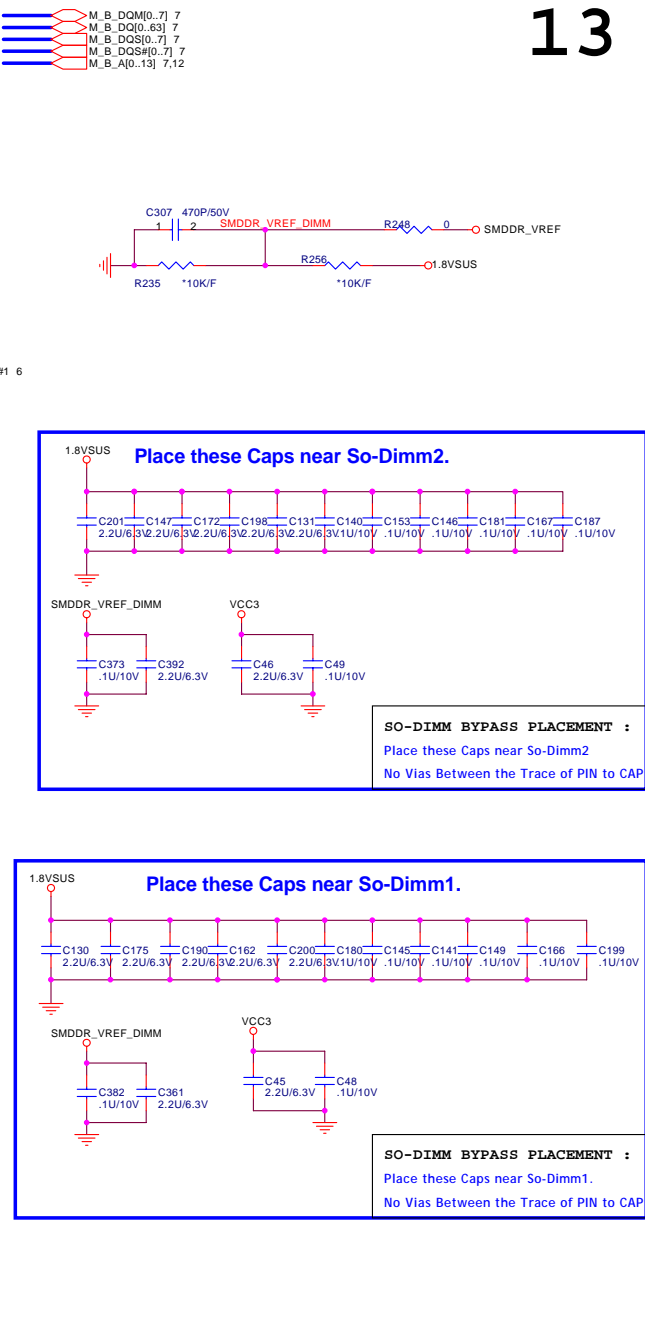
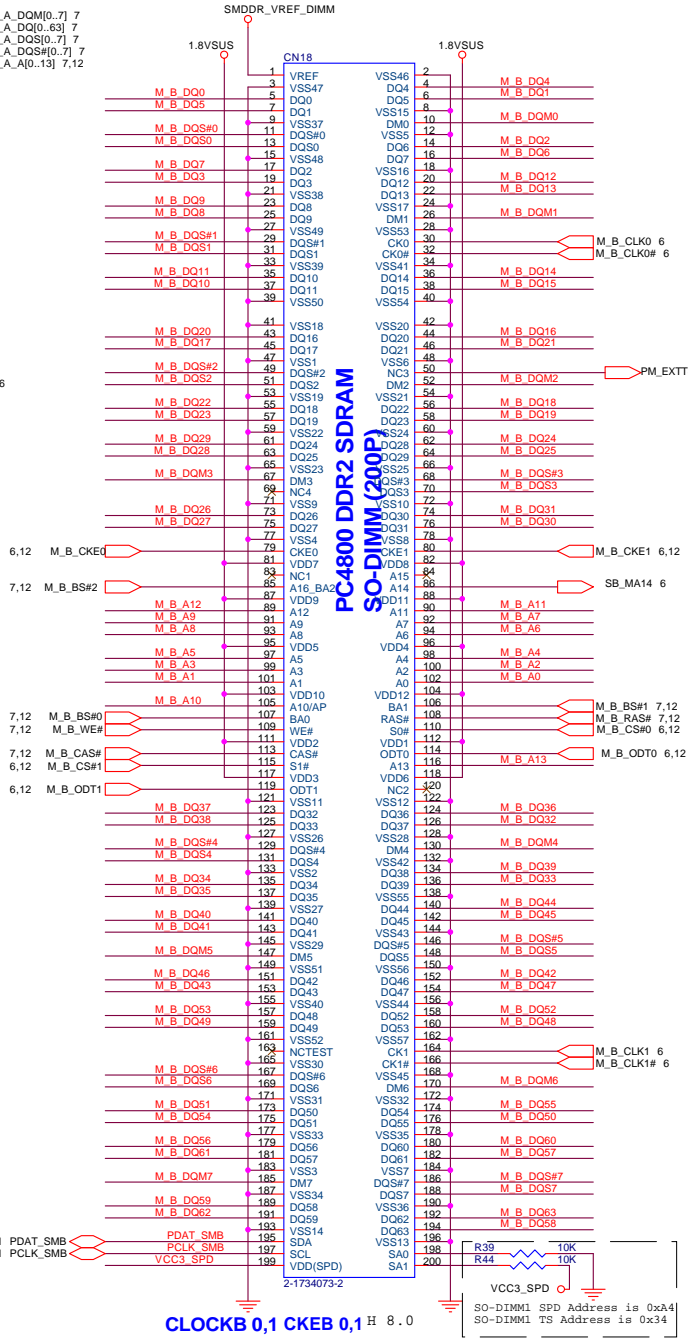
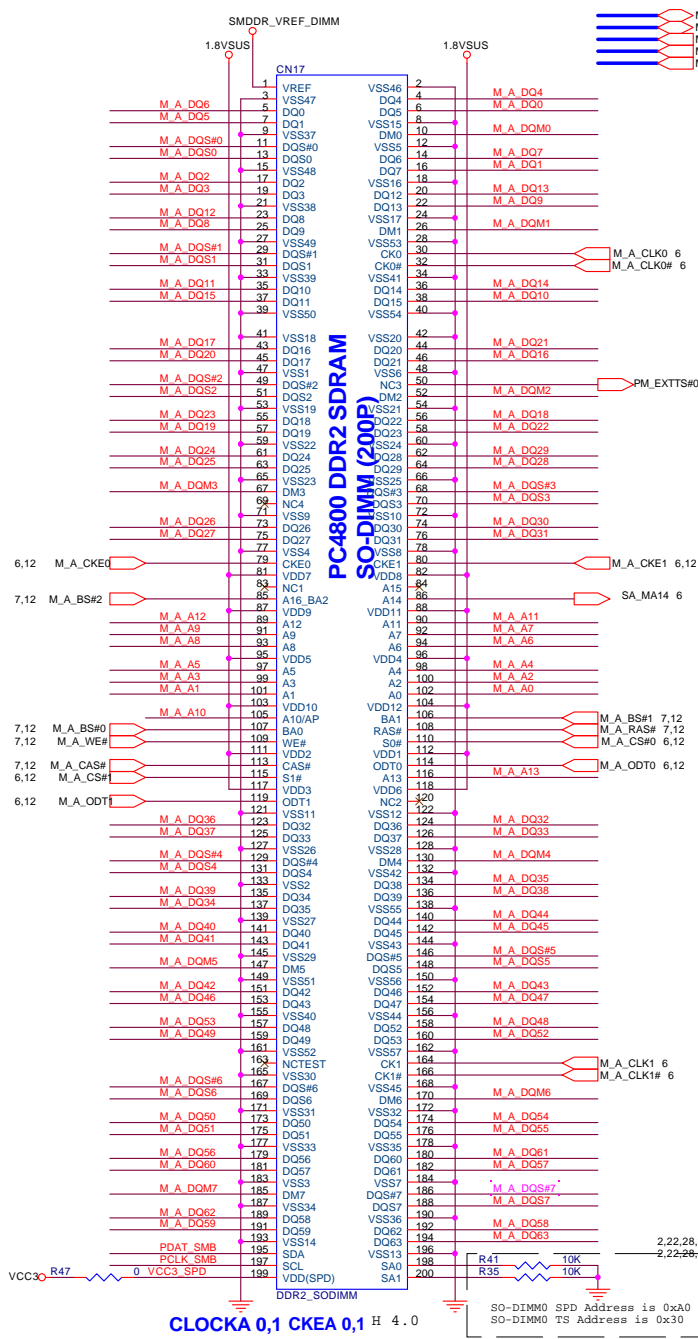


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

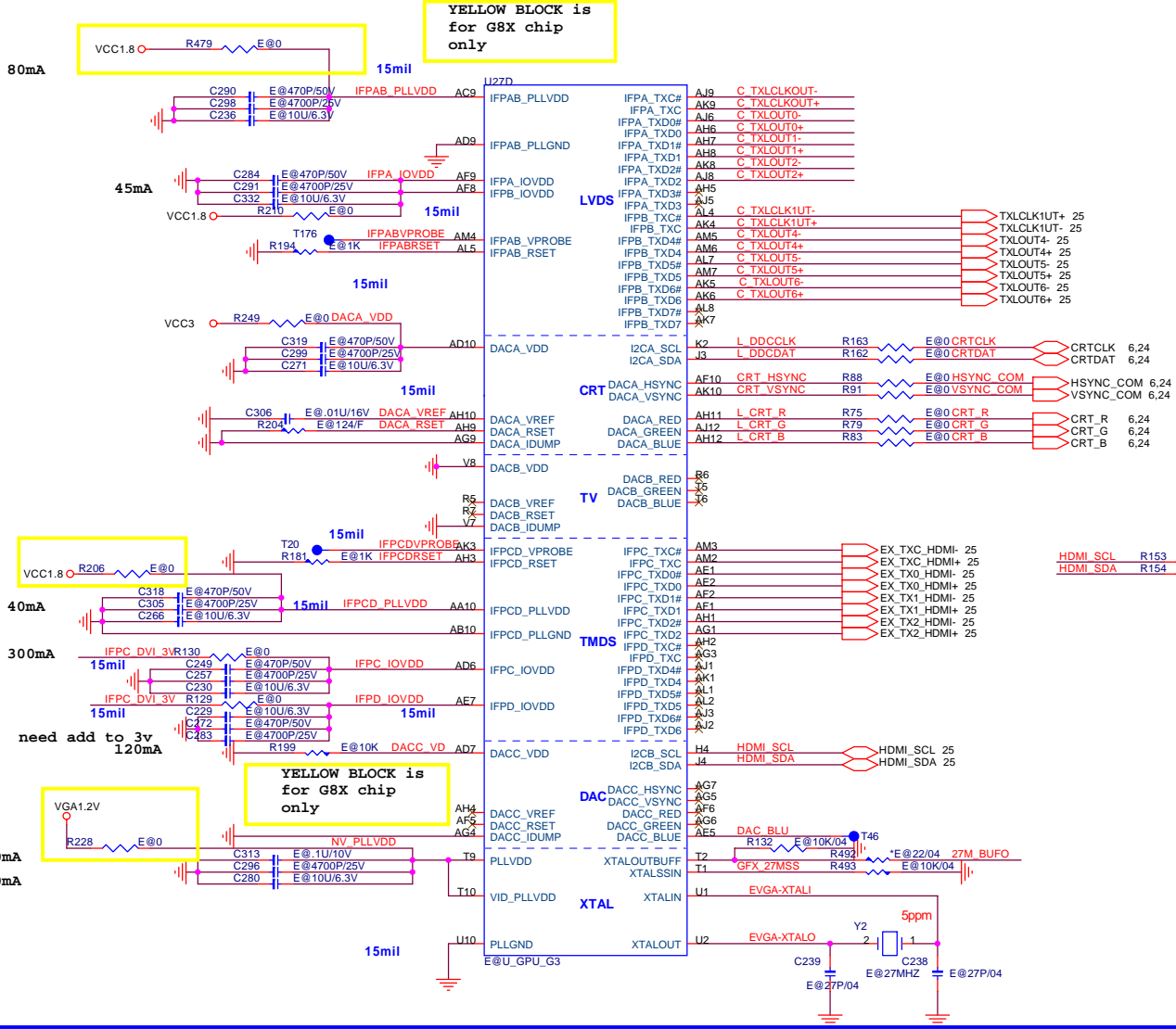


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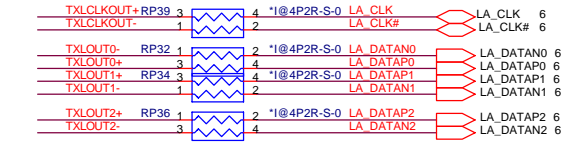
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| Size | Document Number | Rev |
| | DDR2 | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 12 of 46 |



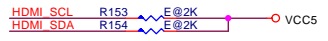
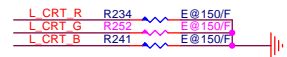
hexainf@hotmail.com



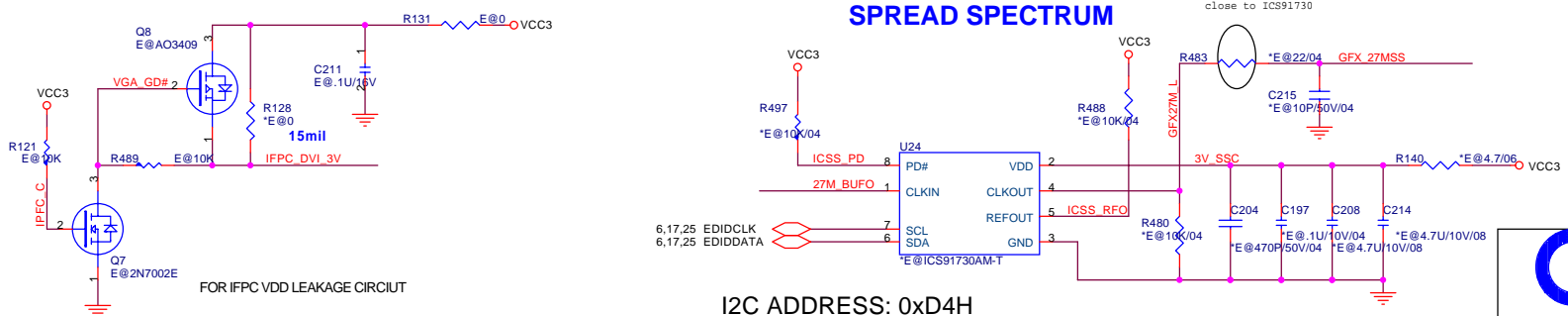
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA



SPREAD SPECTRUM



I2C ADDRESS: 0xD4H

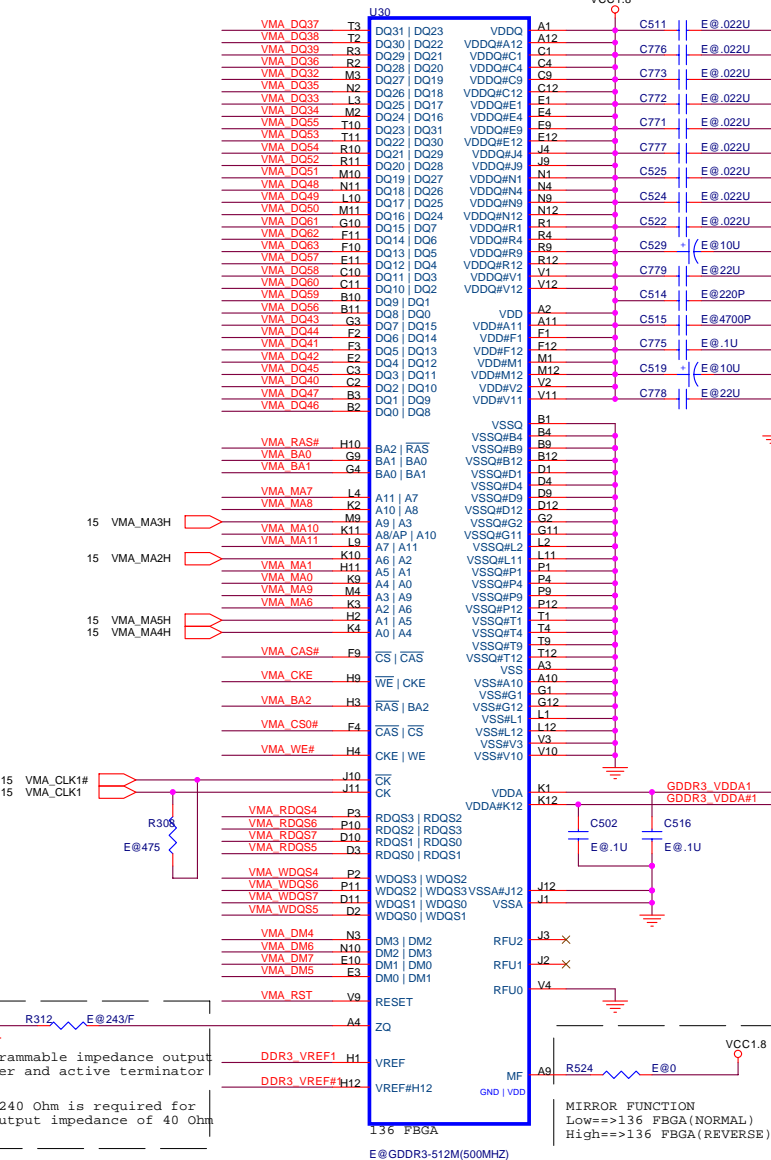
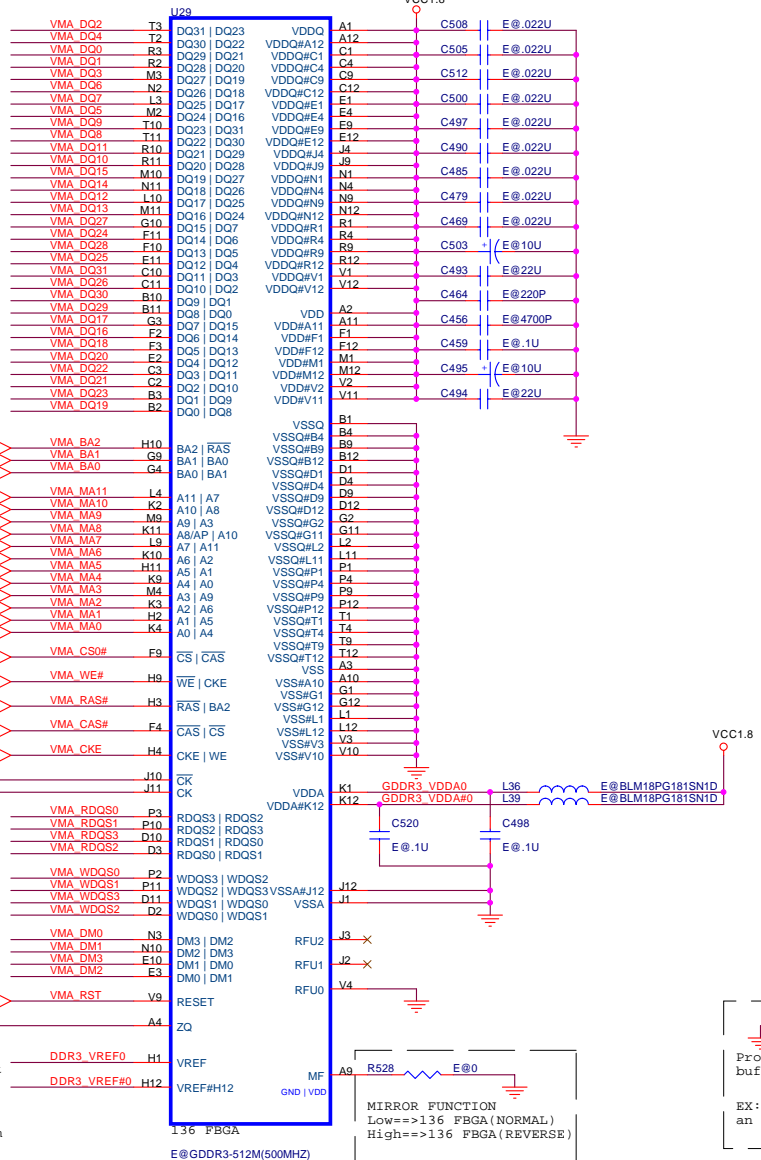
When use internal spread spectrum, this part not stuff

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| Size | Document Number | Rev |
| | VGA | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 16 of 46 |

External VGA Memory

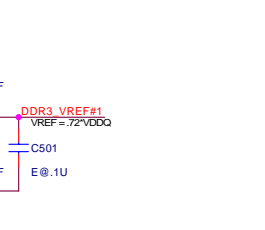
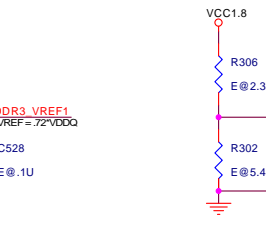
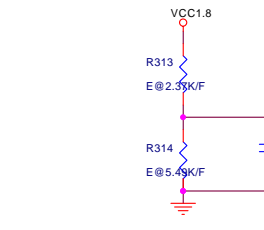
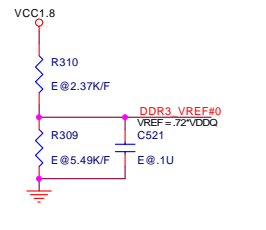
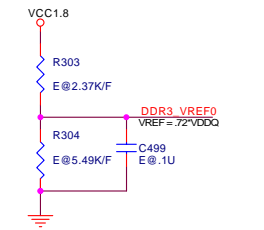
256/512 Mbit GDDR3 Channels



Programmable impedance output buffer and active terminator
EX: 240 Ohm is required for an output impedance of 40 Ohm

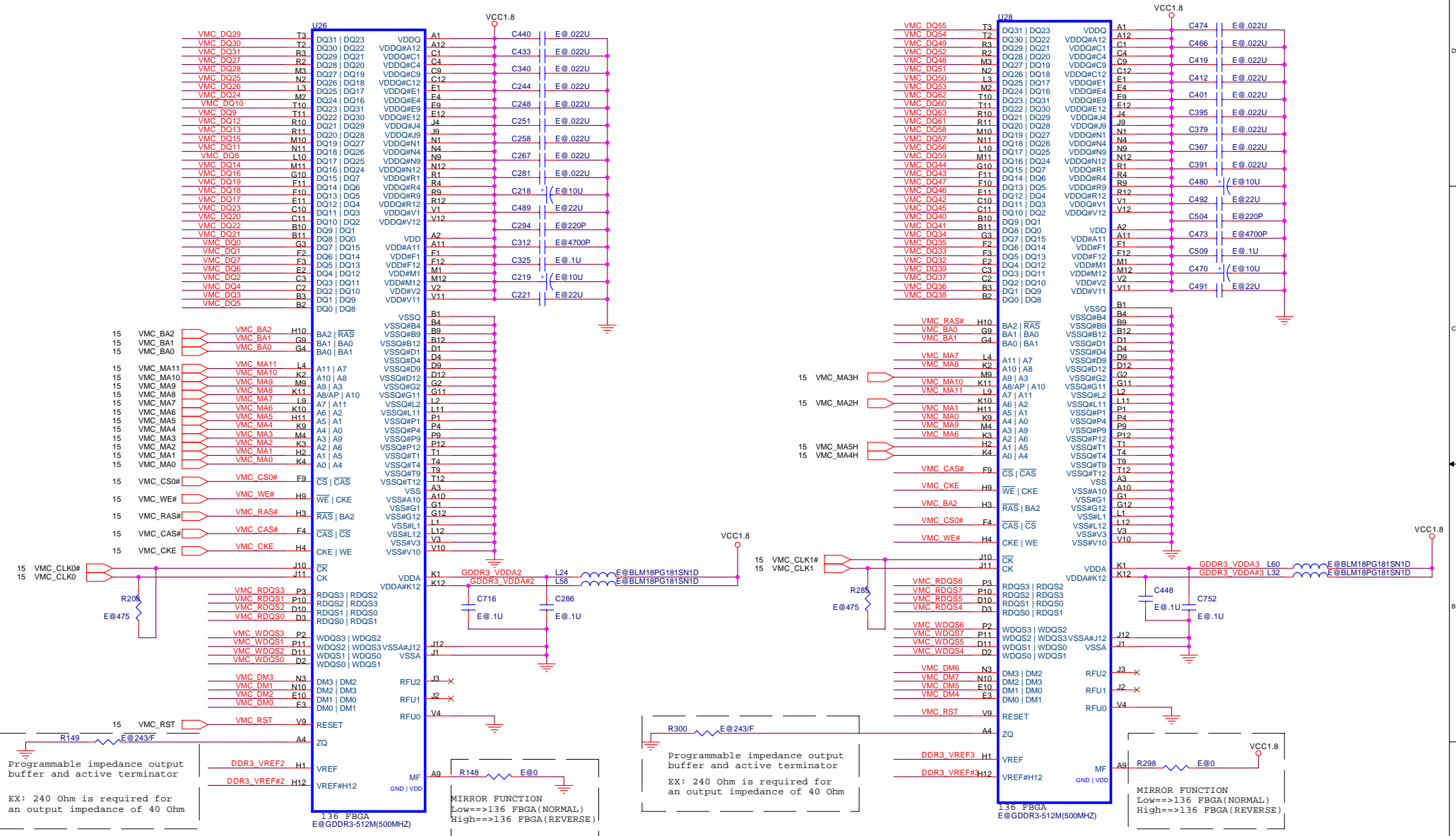
Programmable impedance output buffer and active terminator
EX: 240 Ohm is required for an output impedance of 40 Ohm

Programmable impedance output buffer and active terminator
EX: 240 Ohm is required for an output impedance of 40 Ohm



External VGA Memory

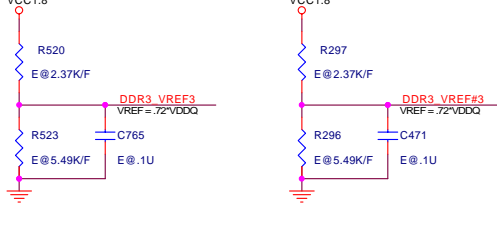
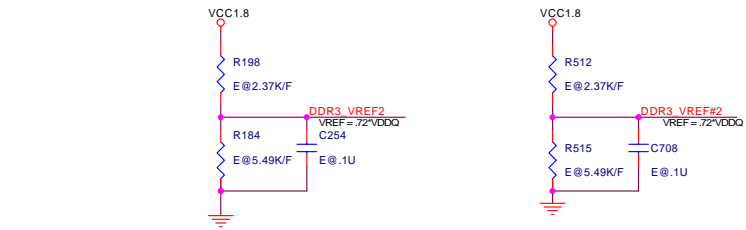
256/512 Mbit GDDRIII Channels



Programmable impedance output buffer and active terminator
EX: 240 Ohm is required for an output impedance of 40 Ohm

Programmable impedance output buffer and active terminator
EX: 240 Ohm is required for an output impedance of 40 Ohm

MIRROR FUNCTION
Low==>136 FBGA(NORMAL)
High==>136 FBGA(REVERSE)

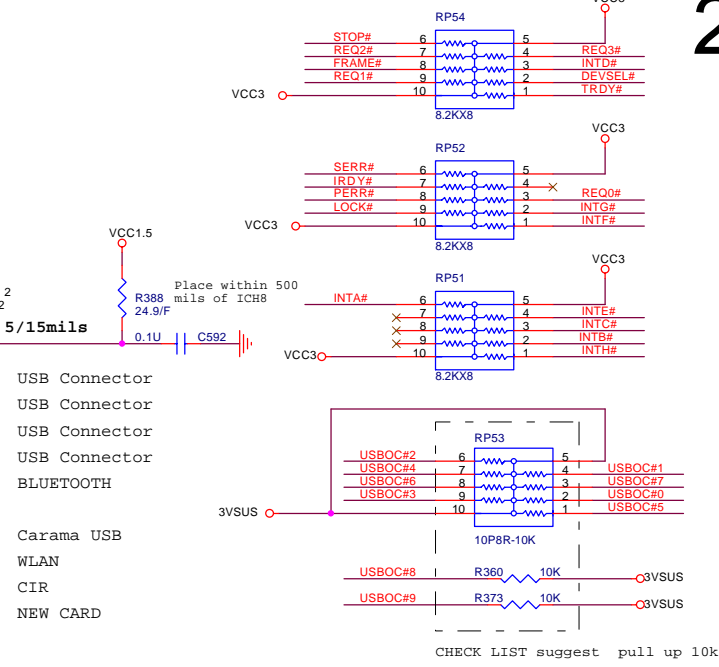
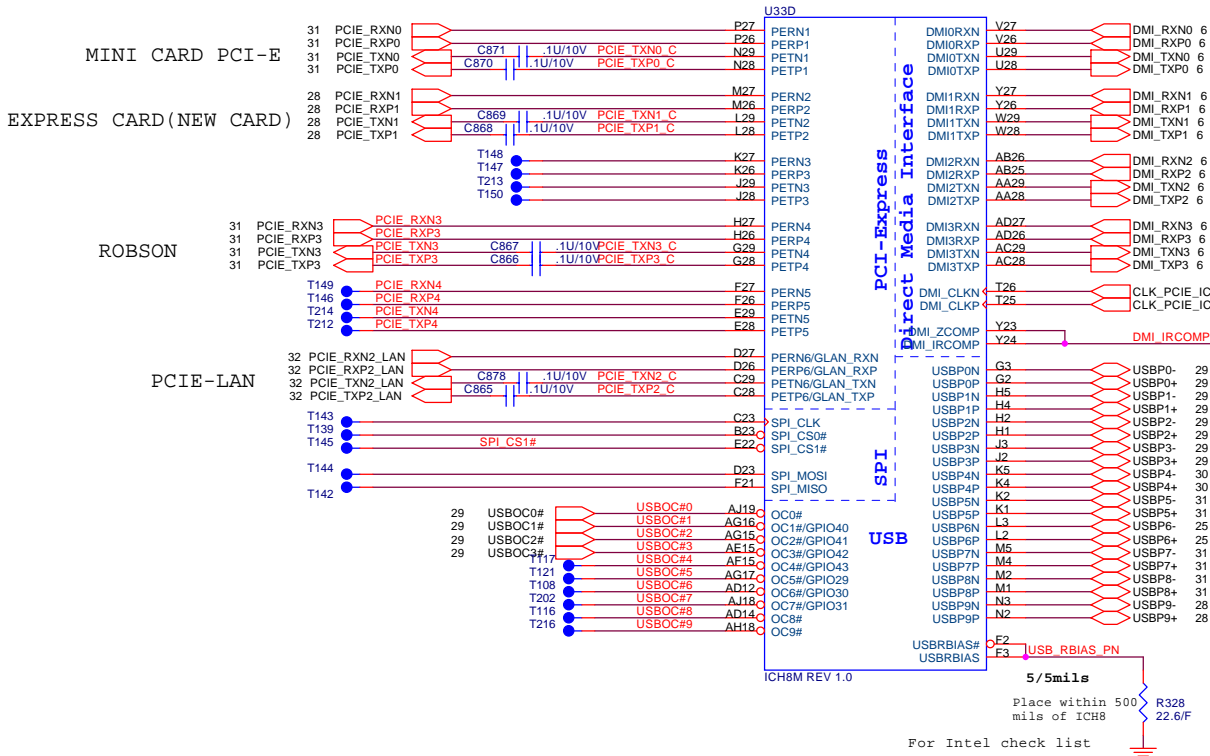


Update to 1.8V for reverse config. nicole 10/9

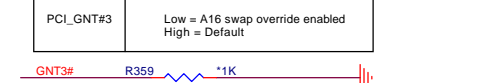
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| | | |
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| Size | Document Number | Rev |
| | NVG73M VRAM-2 (GDDR3) | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 19 of 46 |

txemail@hotmail.com



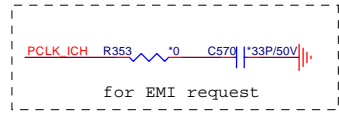
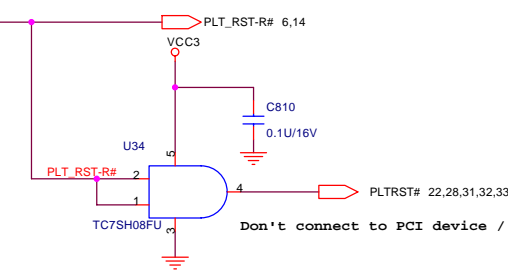
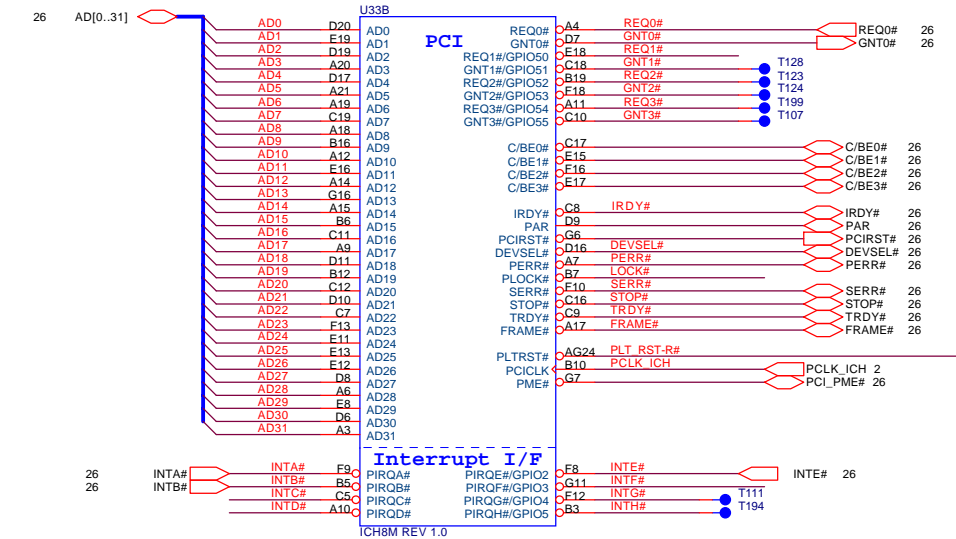
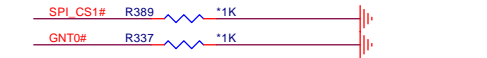
A16 SWAP Override strap



ICH8 Boot BIOS select

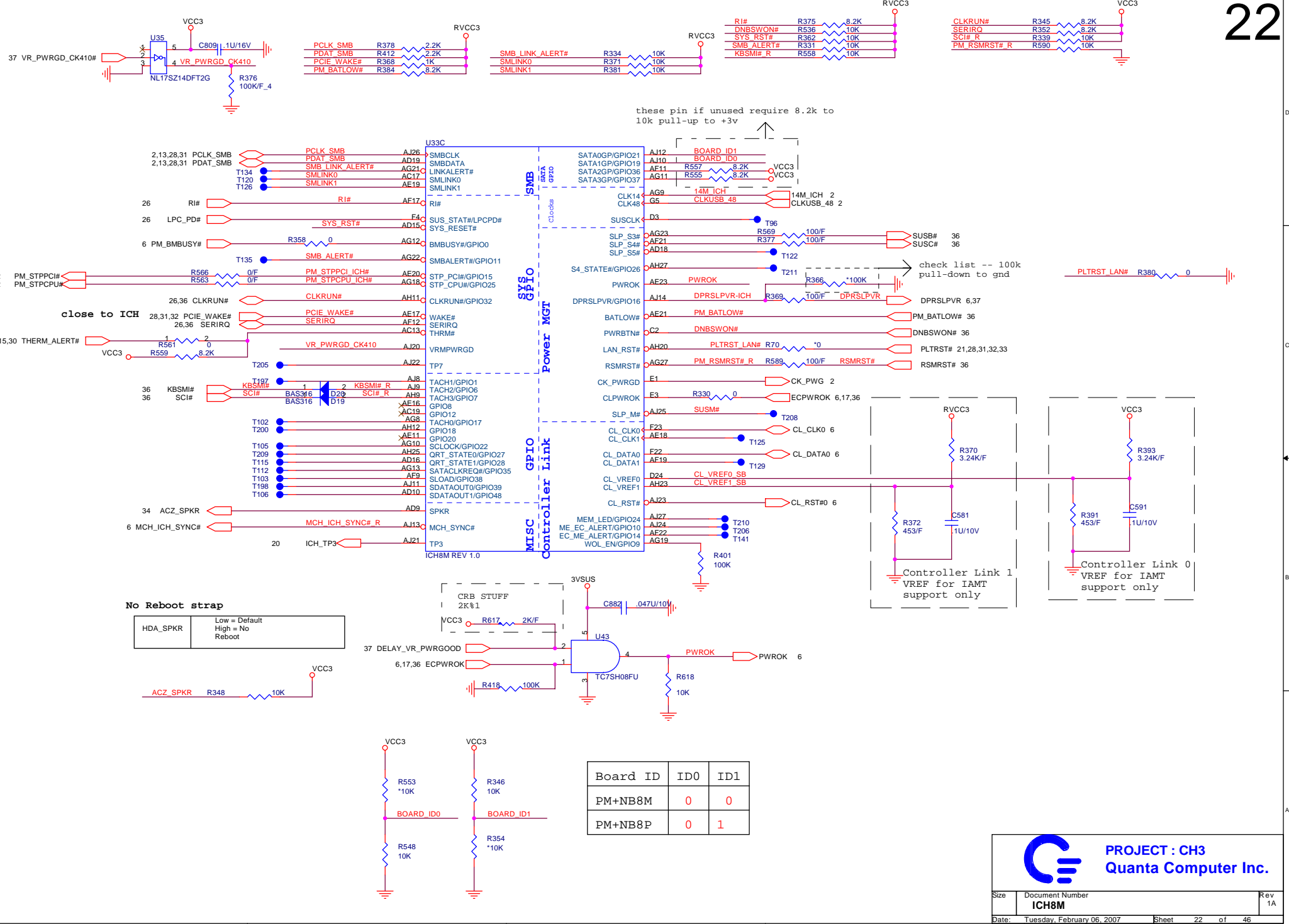
| PCI_GNT#0 | SPI_CS#1 | Boot BIOS Location |
|-----------|----------|--------------------|
| 0 | 1 | SPI |
| 1 | 0 | PCI |
| 1 | 1 | LPC(Default) |

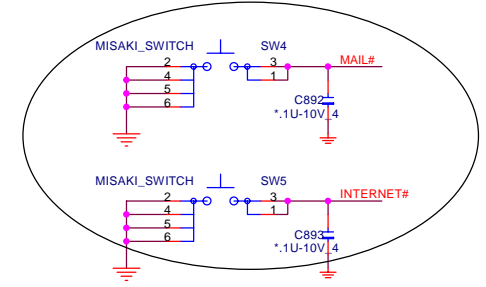
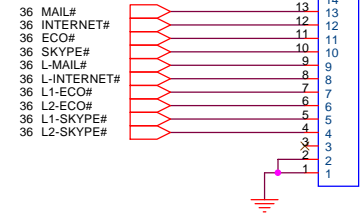
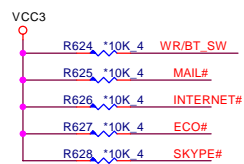
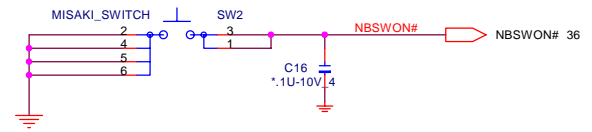
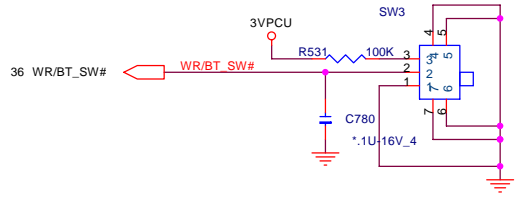
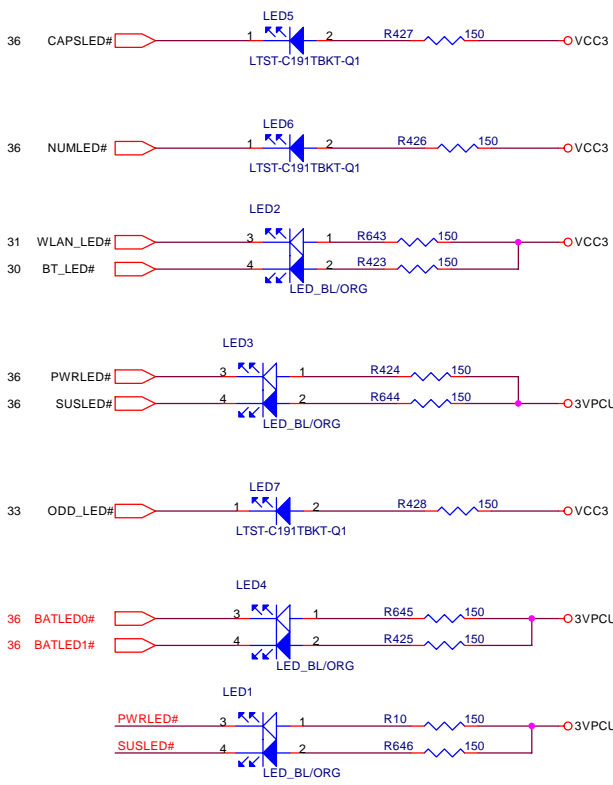
Update Nicole 9/25



PROJECT : CH3
Quanta Computer Inc.

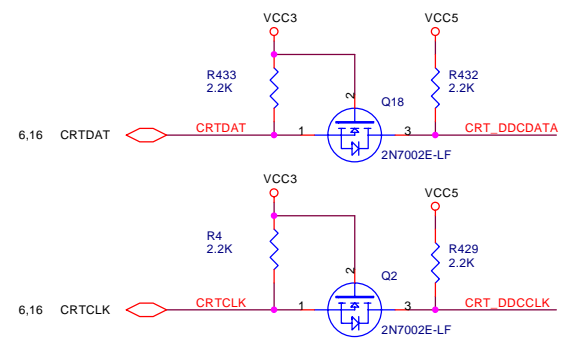
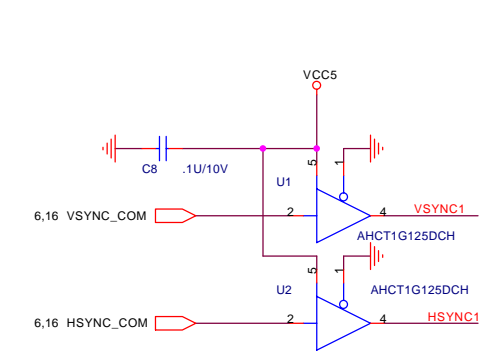
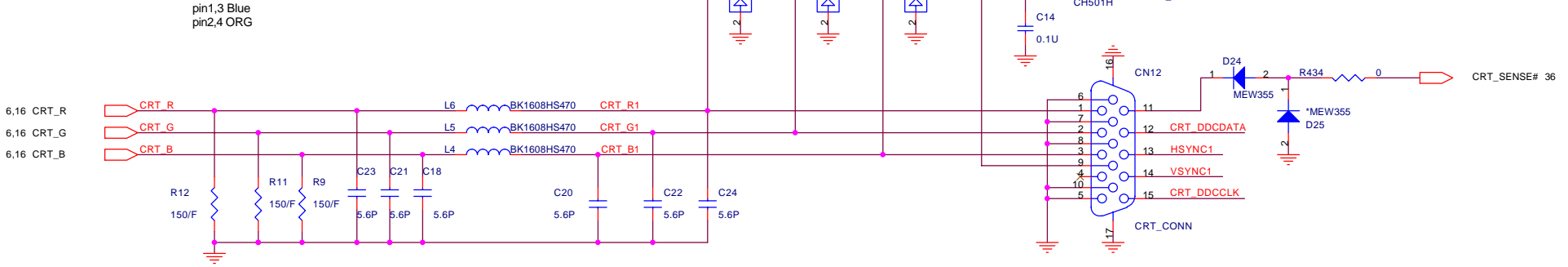
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|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | ICH8M | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 21 of 46 |



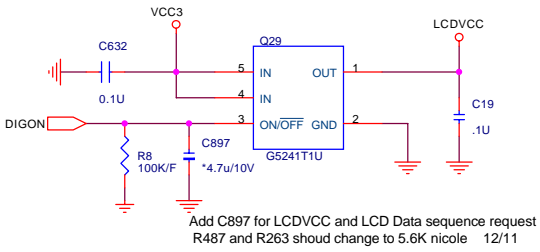


SW4, SW5 not stuff in NEC control in BOM Nicole 11/08

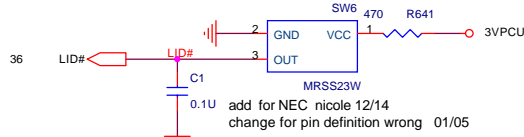
for BenQ SW4 used as SRS function, SW5 used as Snapshot. need EC code. from SG



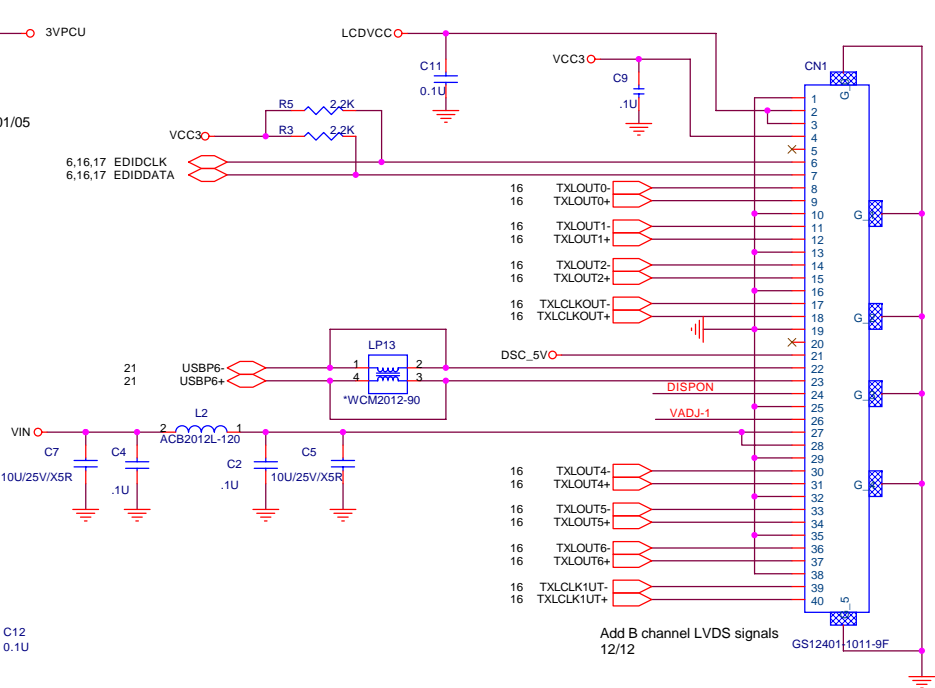
PANEL VCC CONTROL



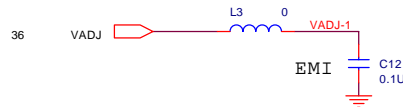
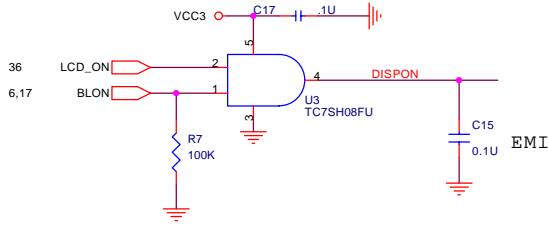
LID



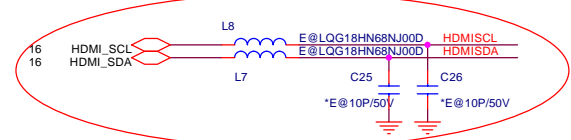
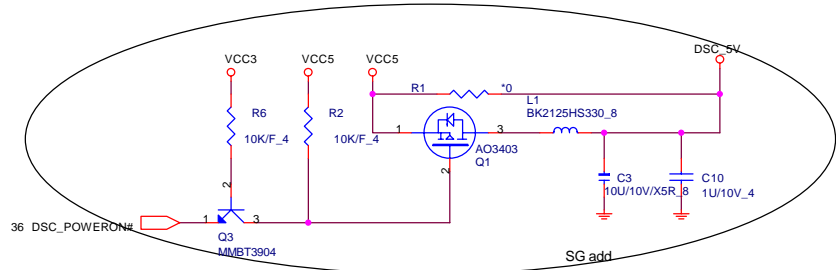
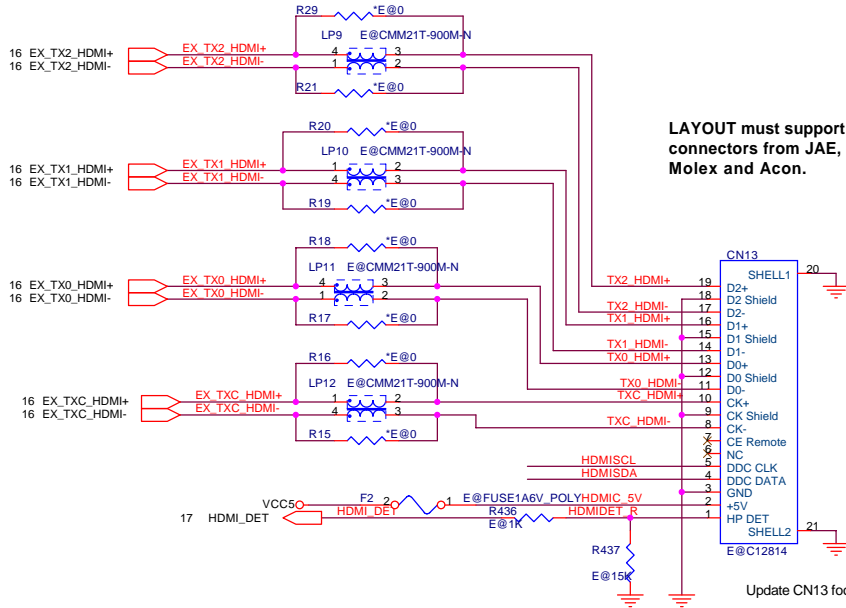
LCD CONNECTOR



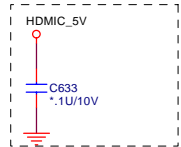
BACKLIGHT CONTROL




HDMI PORT



For HDMI Nvidia's PUN issue





PROJECT : CH3
LCD /CAMERA

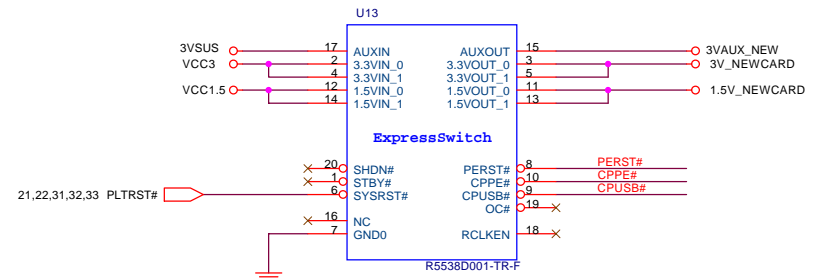
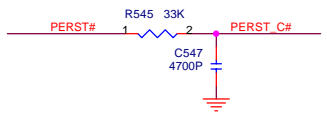
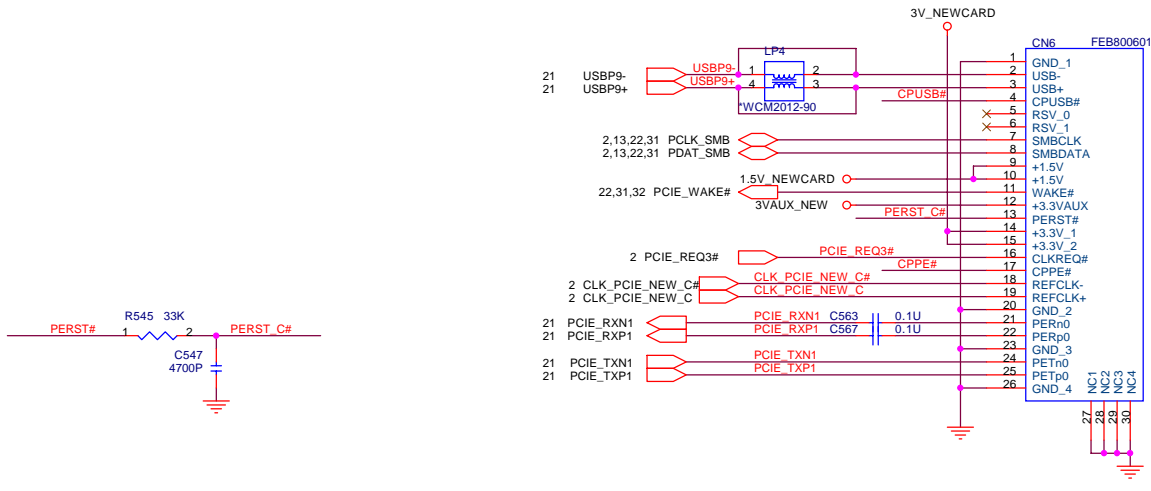
| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| Date: | Tuesday, February 06, 2007 | Sheet 25 of 46 |

U32B

| | | |
|---------------|-----|---|
| CAD31 | C10 | X |
| CAD30 | A10 | X |
| CAD29 | E11 | X |
| CAD28 | C11 | X |
| CAD27 | B13 | X |
| CAD26 | E11 | X |
| CAD25 | C13 | X |
| CAD24 | A14 | X |
| CAD23 | B14 | X |
| CAD22 | E14 | X |
| CAD21 | A16 | X |
| CAD20 | D19 | X |
| CAD19 | D19 | X |
| CAD18 | F17 | X |
| CAD17 | H19 | X |
| CAD16 | J17 | X |
| CAD15 | J15 | X |
| CAD14 | J18 | X |
| CAD13 | K15 | X |
| CAD12 | K17 | X |
| CAD11 | K18 | X |
| CAD10 | L15 | X |
| CAD09 | L18 | X |
| CAD08 | L19 | X |
| CAD07 | M17 | X |
| CAD06 | M18 | X |
| CAD05 | M19 | X |
| CAD04 | M15 | X |
| CAD03 | M15 | X |
| CAD02 | N17 | X |
| CAD01 | N18 | X |
| CAD00 | F19 | X |
| CCBE3 | E13 | X |
| CCBE2 | E18 | X |
| CCBE1 | H18 | X |
| CCBE0 | L17 | X |
| RSVD_04/D2 | B10 | X |
| CCD1#/CD1# | N15 | X |
| CCD2#/CD2# | B11 | X |
| CVS1/VS1# | A13 | X |
| CRST# | C15 | X |
| CBLOCK# | H15 | X |
| CREQ#/INPACK# | C14 | X |
| CSERR#/WAIT# | C12 | X |
| CDEVSEL# | F19 | X |
| CFRAME# | E19 | X |
| CGRANT# | G17 | X |
| CINT# | E12 | X |
| CVS2/VS2# | B16 | X |
| CPERR# | G19 | X |
| CSTOP# | G19 | X |
| CIRDY | F17 | X |
| CTRDY# | G15 | X |
| RSVD_02/A18 | H17 | X |
| RSVD_01/D14 | M19 | X |
| CCLKRUN# | A11 | X |
| CPAR | H14 | X |
| VCCA_01 | A15 | X |
| VCCA_00 | J19 | X |
| CSTSCHG | A12 | X |
| CAUDIO | B12 | X |
| CCLK | F18 | X |

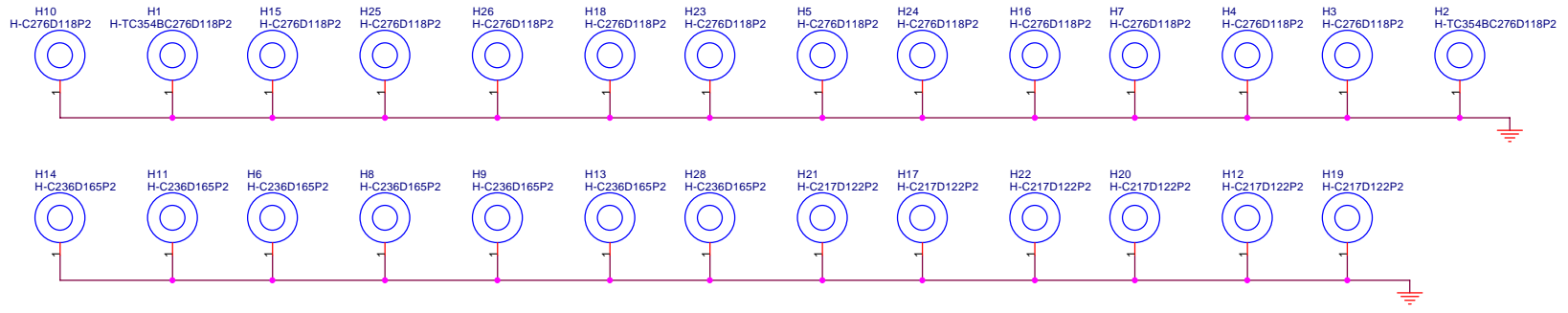
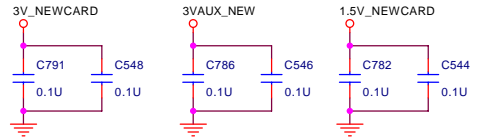
CardBus Interface

PC18402



SHDN#, STBY#, PERST# and CPPE# have internal pull-up to AUXIN.
So del R551, R541, R327, R329 nicole 12/11

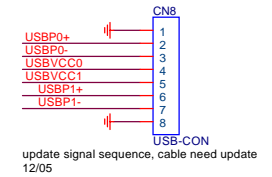
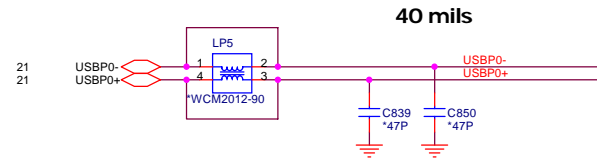
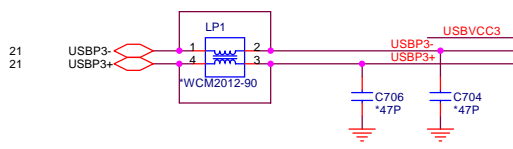
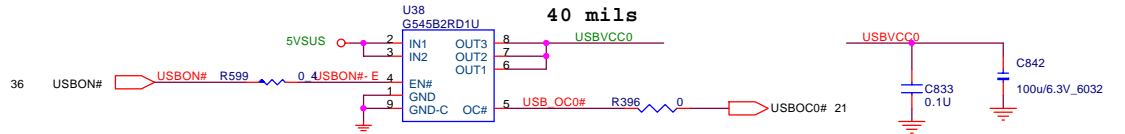
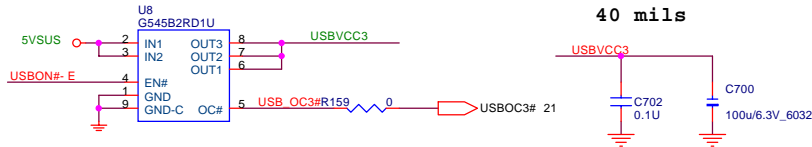
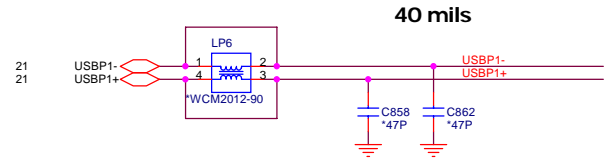
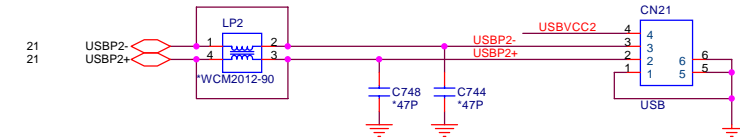
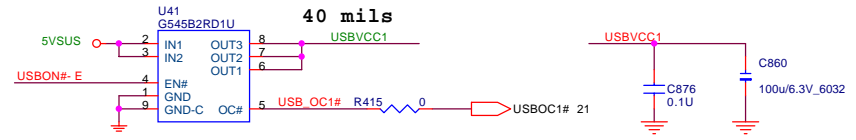
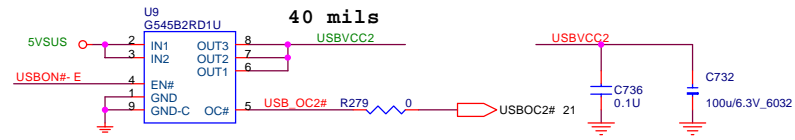
Del R532 and R556 nicole 12/11



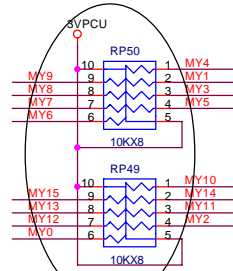
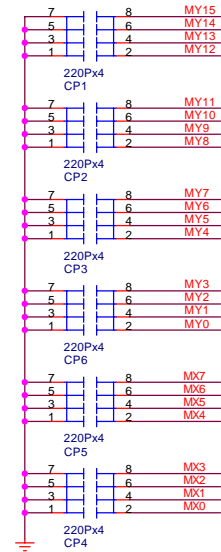
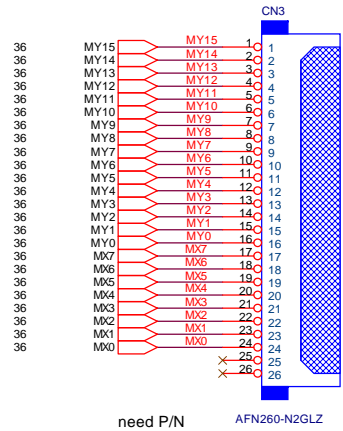
PROJECT : CH3
Quanta Computer Inc.

| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | NEWCARD/HOLE | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 28 of 46 |

USB PORT



INT Keyboard



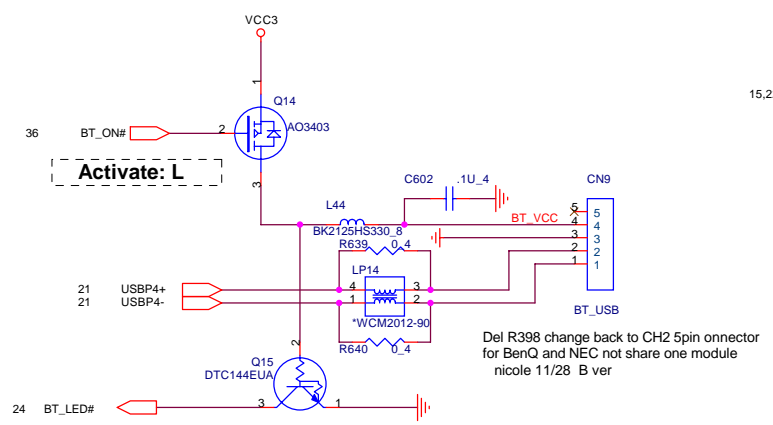
DEL MX[7:0] pull-up to 3VPCU nicole 9/25

PROJECT : CH3
Quanta Computer Inc.

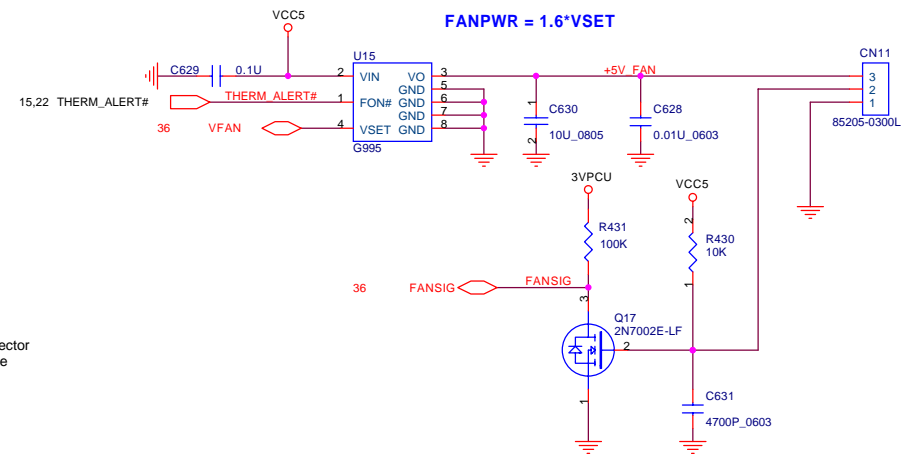
Size: Document Number
KB / USB

Date: Tuesday, February 06, 2007 Sheet 29 of 46 Rev 1A

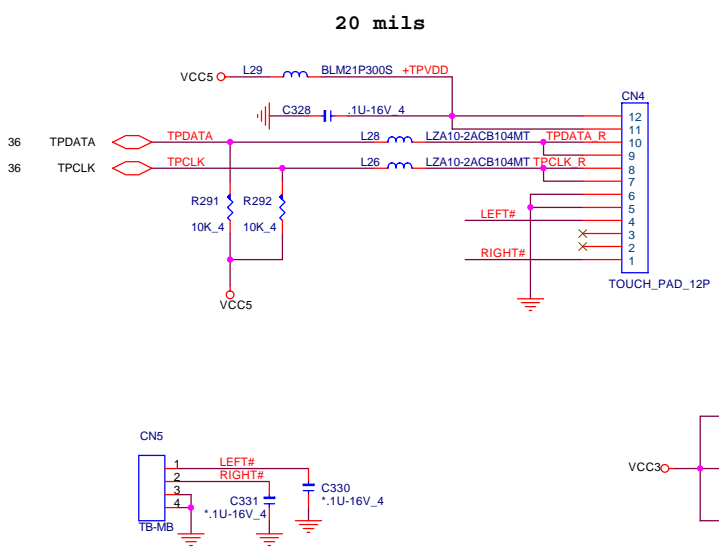
BT Connector



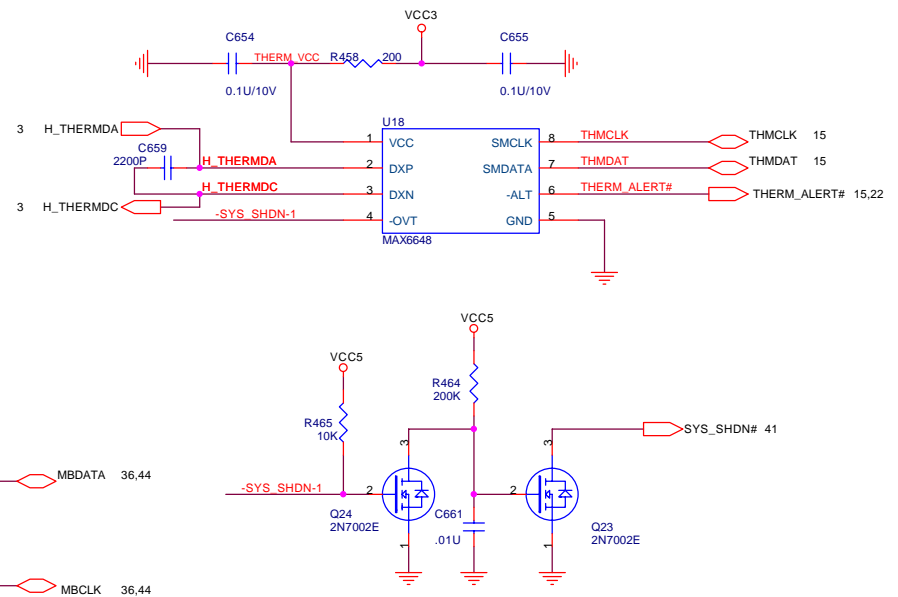
FAN CONN

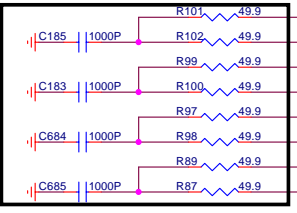
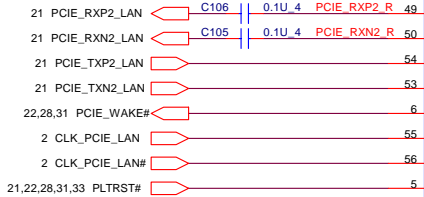
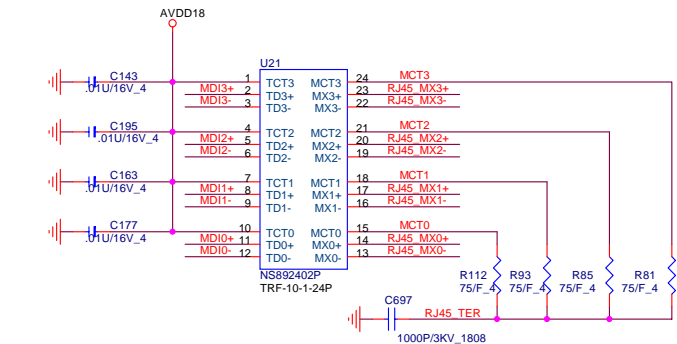
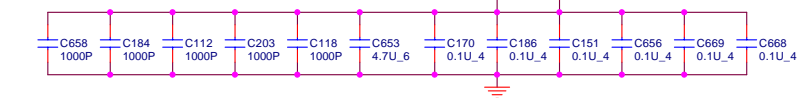
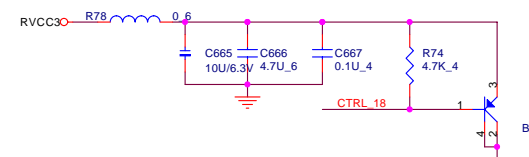
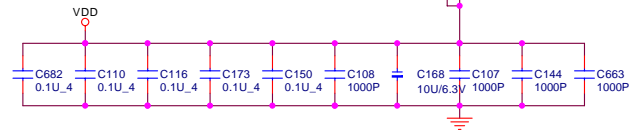
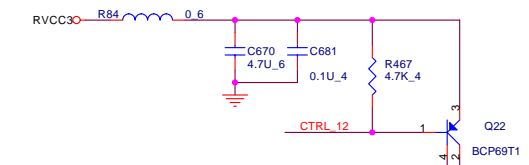
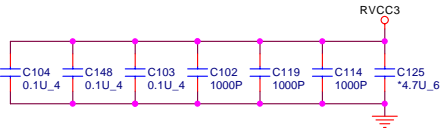
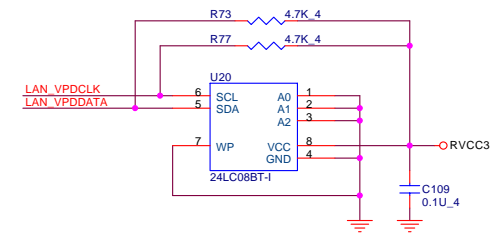


TOUCH PAD

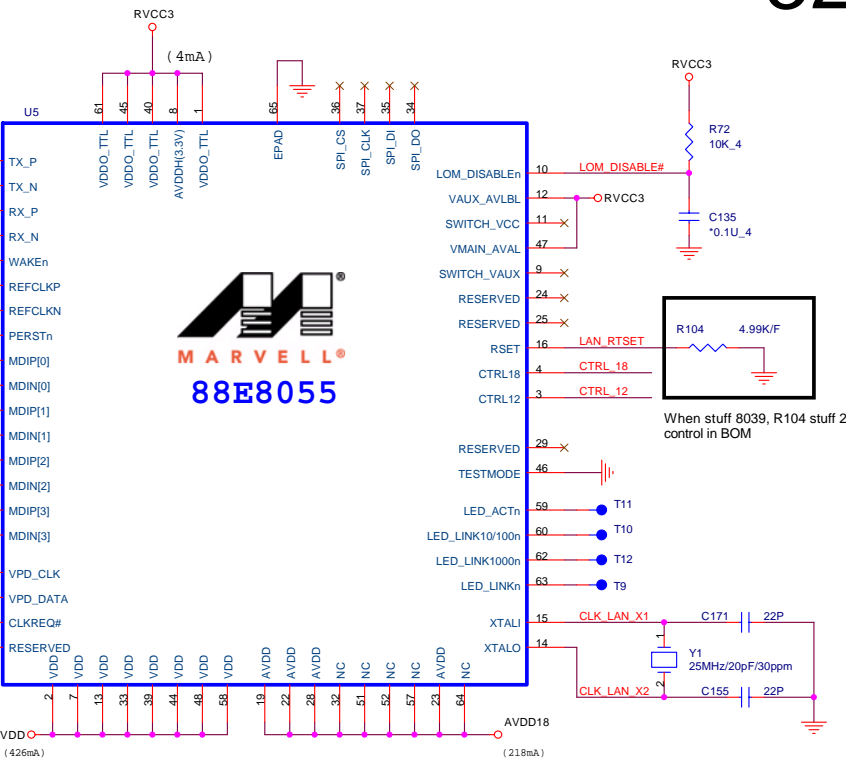


Thermal Sensor





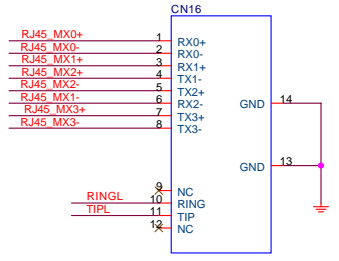
Closed Transformer



Giga: P/N: AJ080550011

pin32, 51, 52, 57 64 and 19,22,23 are 2.5V power

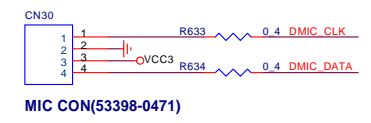
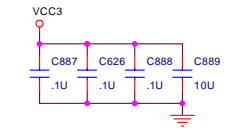
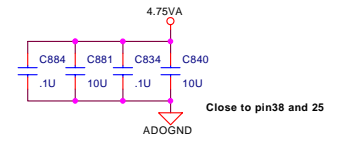
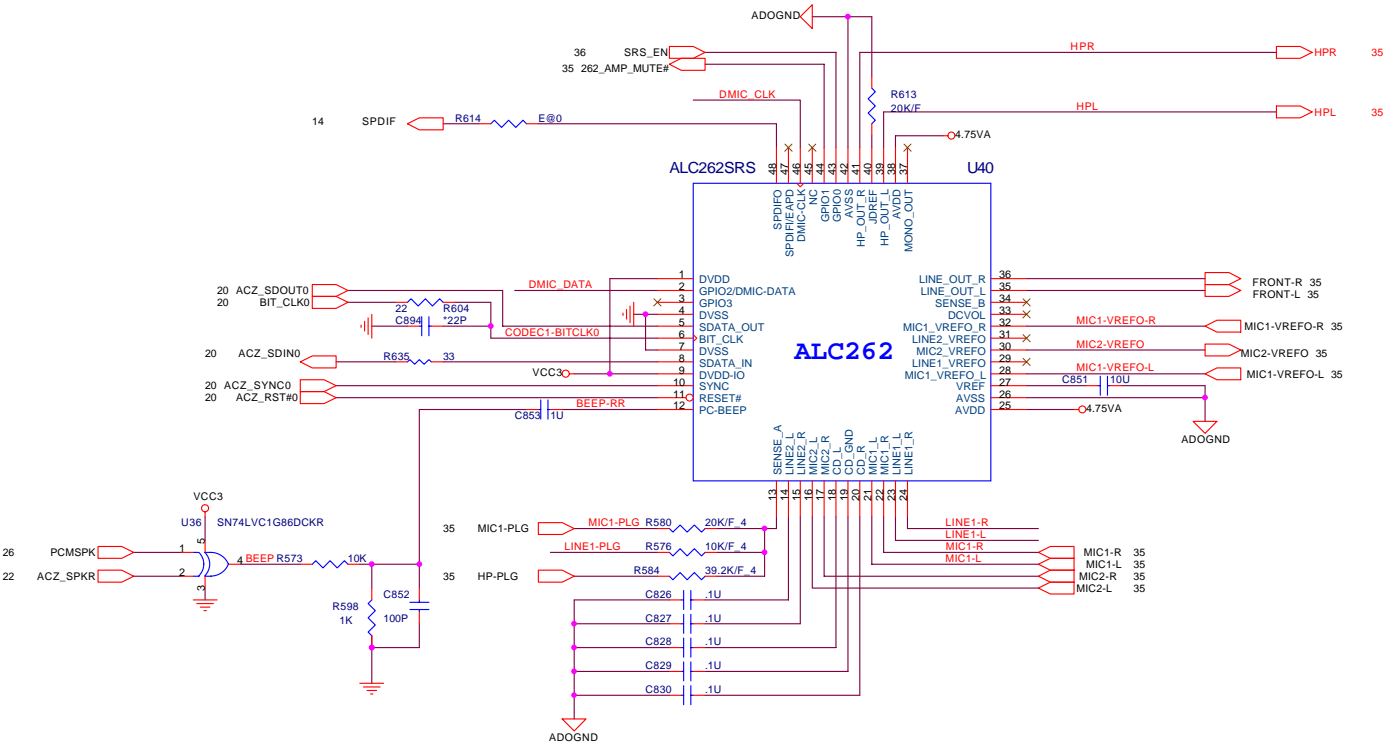
When stuff 8039, R104 stuff 2.0K control in BOM



NEED CHECK

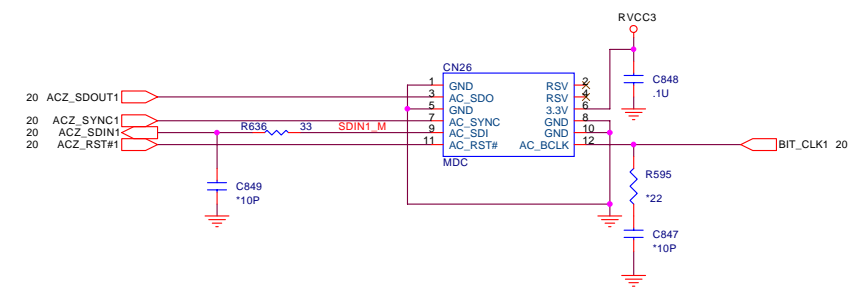


1G -- FCE NS892402P DB0ZH1LAN06
 10/100 -- FCE NS892404 DBED21LAN05

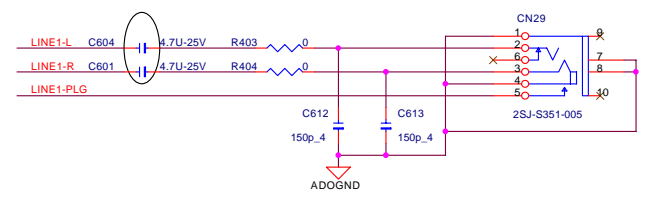


Add digital MIC nicote 12/01

For MDC Module



LINE-IN

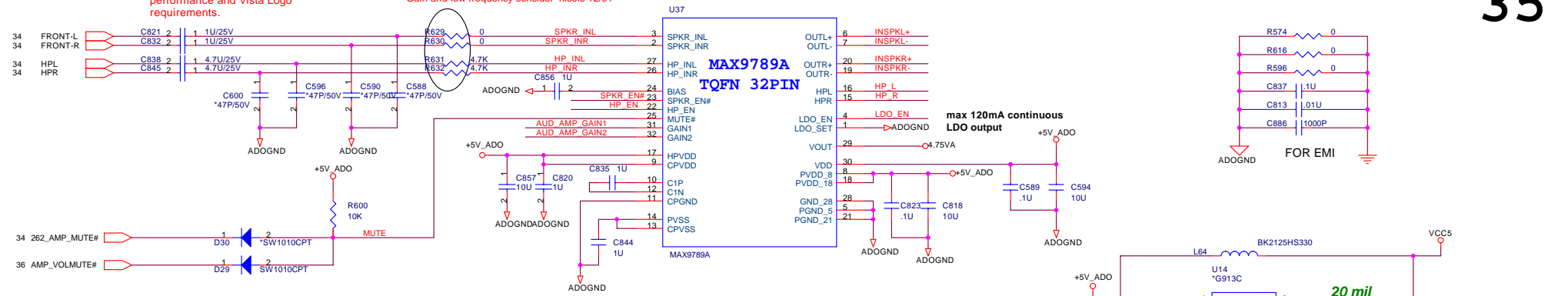


PROJECT : CH3
Quanta Computer Inc.

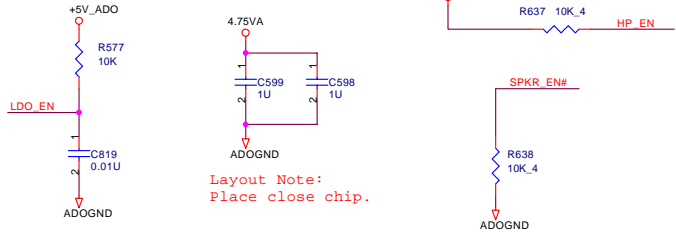
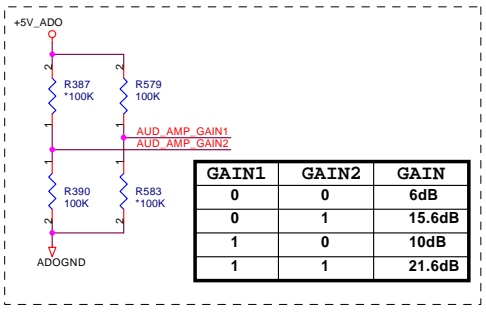
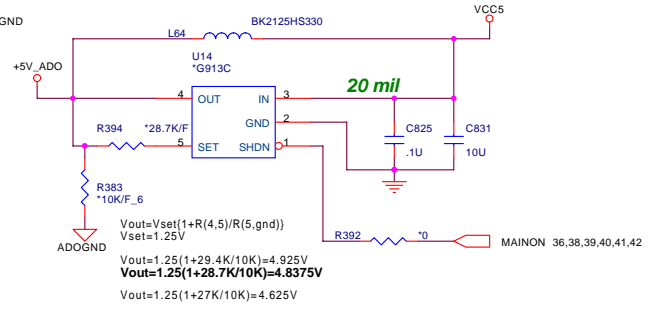
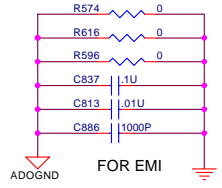
| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | ALC262/MIC/LINE/MDC | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 34 of 46 |

Package 1206 for THD+N performance and Vista Logo requirements.

Add for Realtek AE suggestion Gain and low frequency consider nicole 12/01

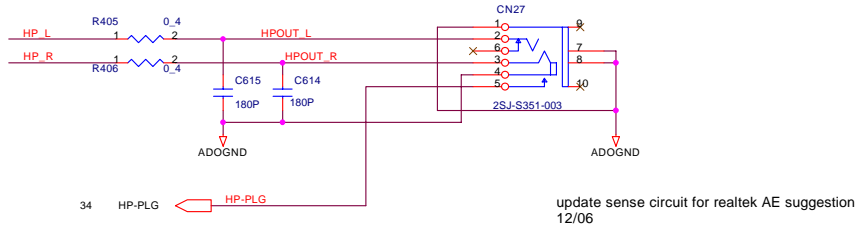


| GAIN1 | GAIN2 | GAIN |
|-------|-------|--------|
| 0 | 0 | 6dB |
| 0 | 1 | 15.6dB |
| 1 | 0 | 10dB |
| 1 | 1 | 21.6dB |



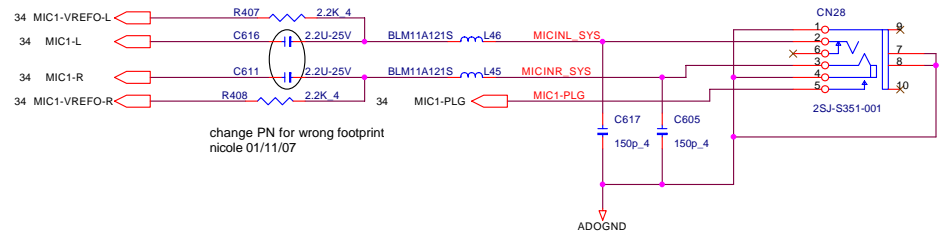
Layout Note: Place close chip.

Headphone out



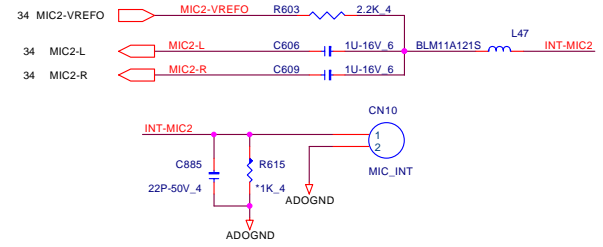
update sense circuit for realtek AE suggestion 12/06

MIC-IN

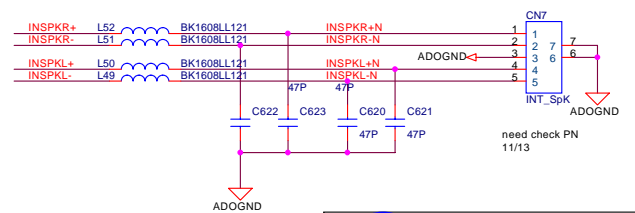


change PN for wrong footprint nicole 01/11/07

INT-MIC



SPEAKER

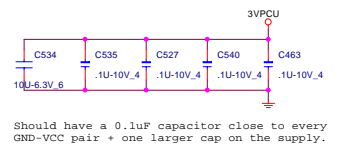
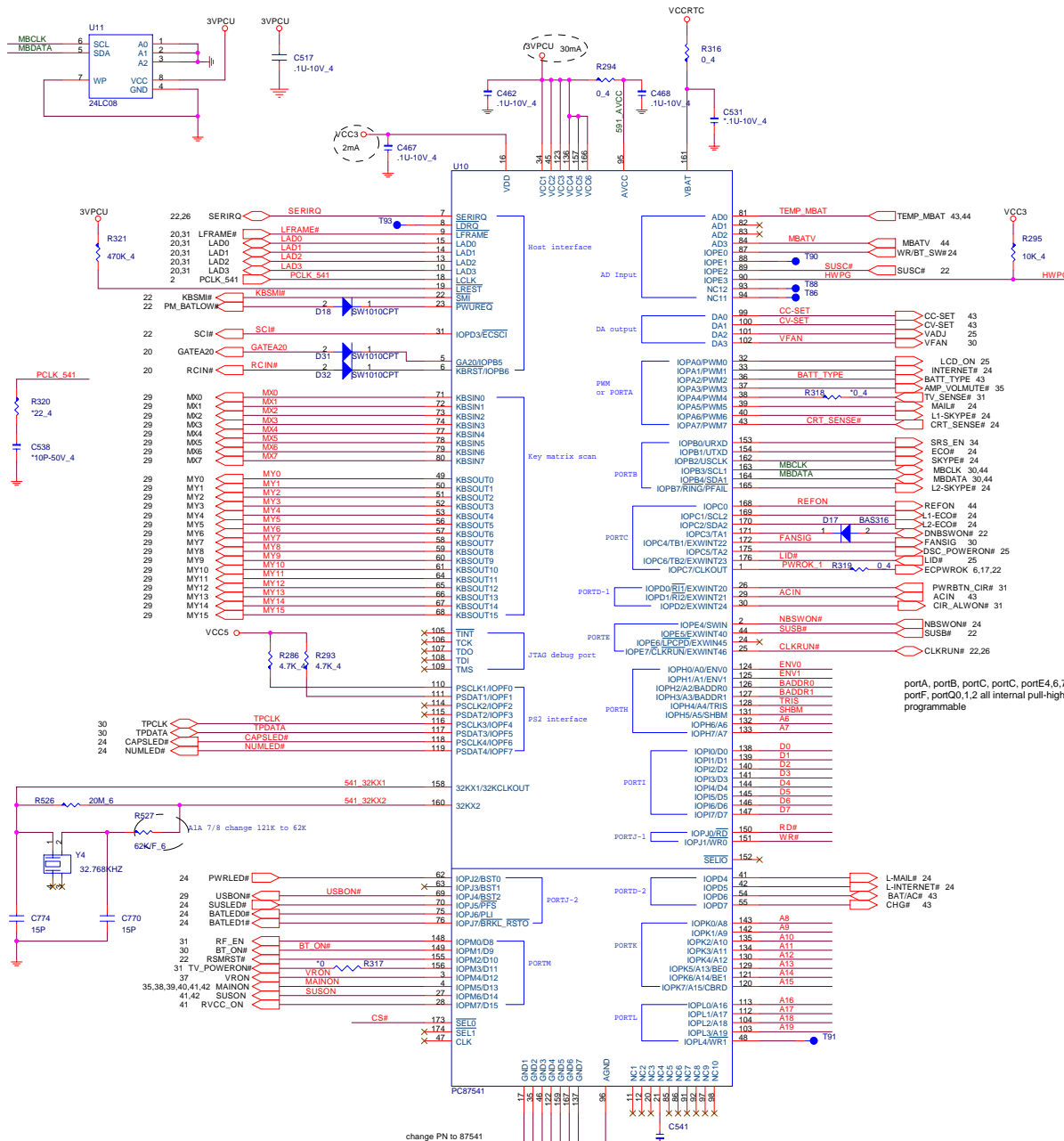


need check PN 11/13

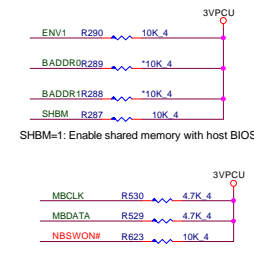
PROJECT : CH3
Quanta Computer Inc.

| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | AMPLIFIER&JACKS | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 35 of 46 |

LDRCQ#(pin 8) internal is no use



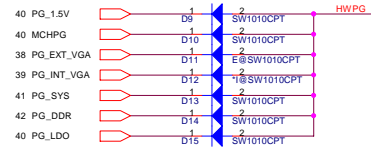
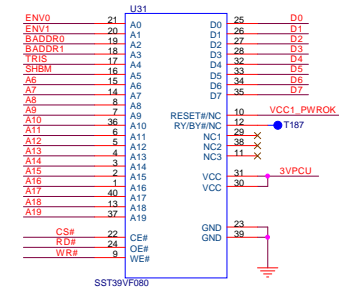
Should have a 0.1µF capacitor close to every GND-VCC pair + one larger cap on the supply.



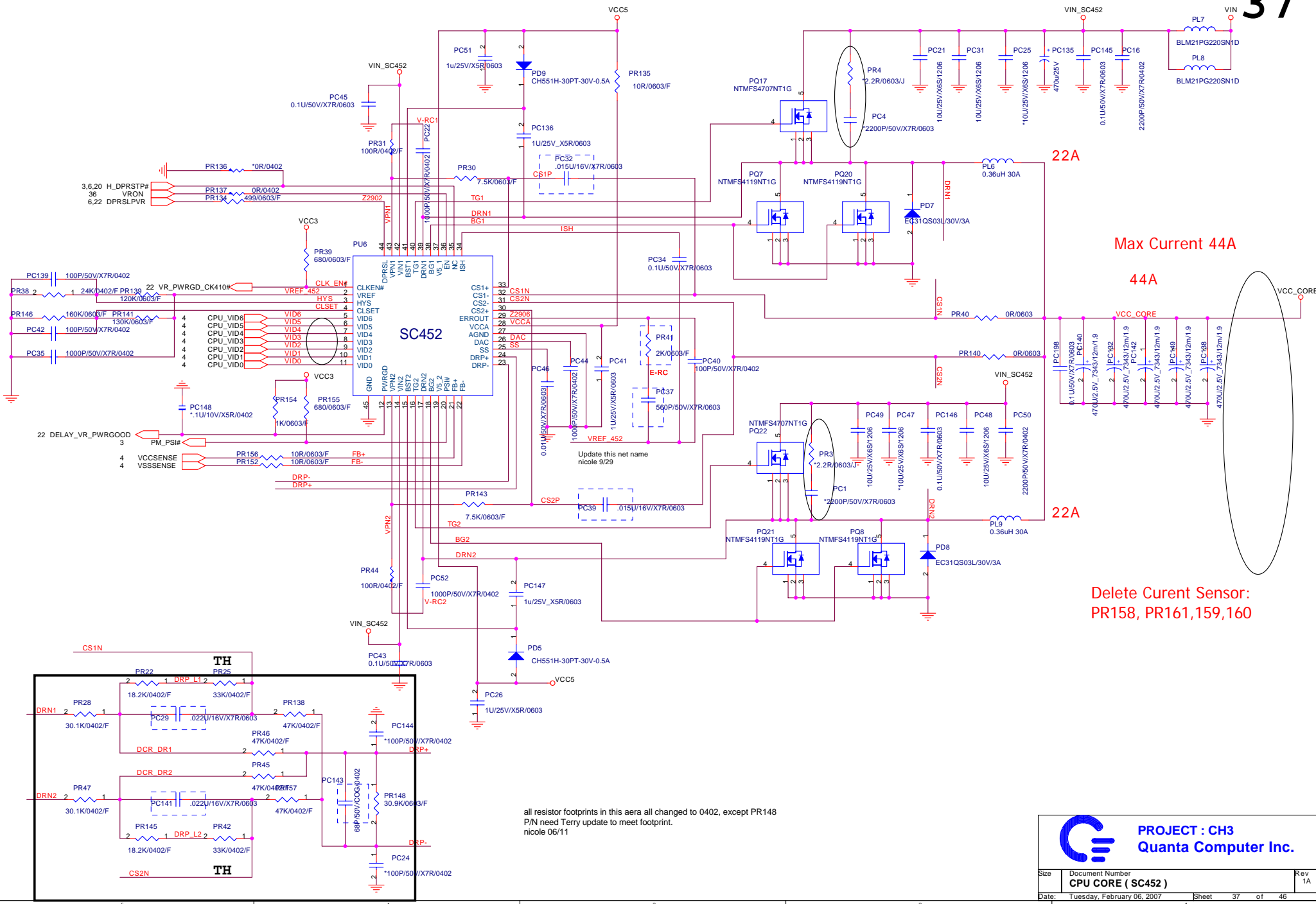
SHBM=1: Enable shared memory with host BIOS

| I/O Address | | Data |
|-------------|--------------------|------------------------|
| BADDR1-0 | Index | 2F |
| 0 0 | 2E | 2F |
| 0 1 | 4E | 4F |
| 1 0 | (HCFGBAH, HCFGBAL) | (HCFGGBAH, HCFGGBAL)+1 |
| 1 1 | | Reserved |

R622,R623, no stuff if is OK can del in B stage




change PN to 87541 nicole 0111107

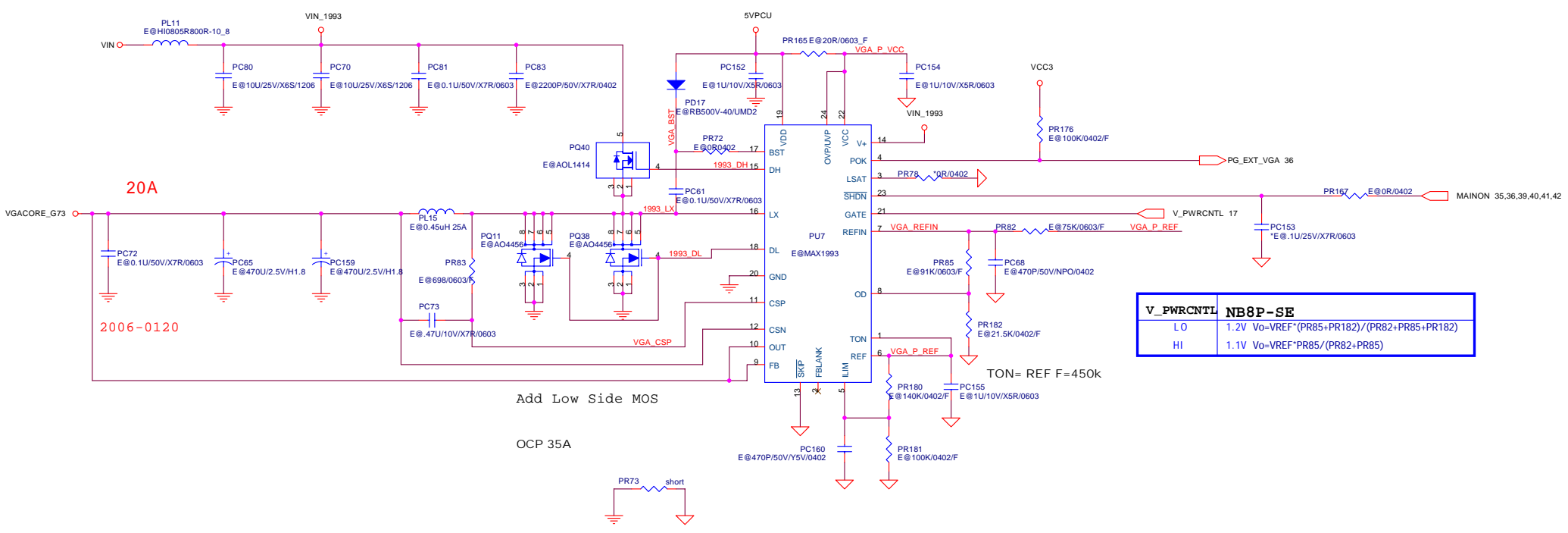


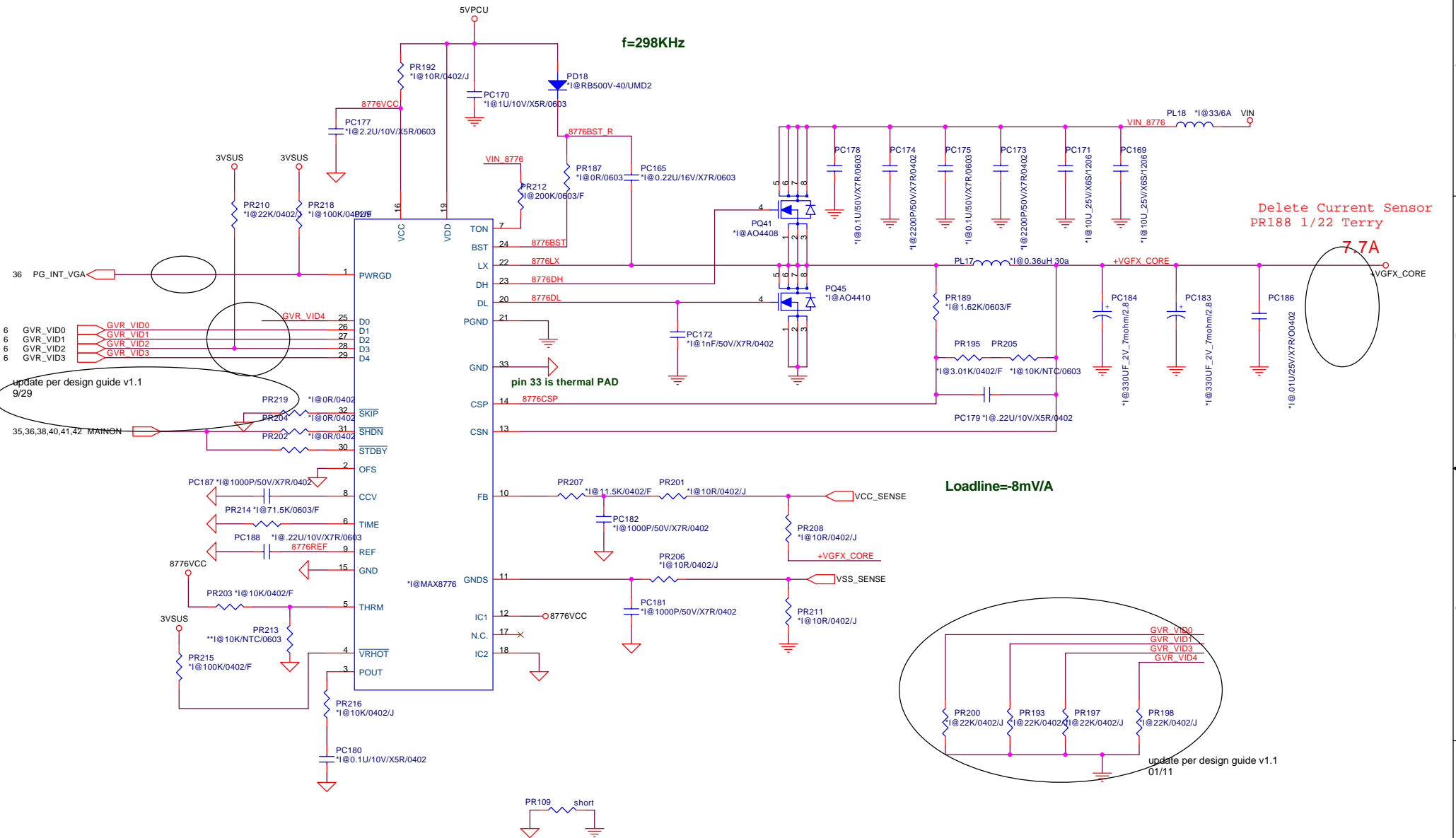
Max Current 44A
44A

Delete Current Sensor:
PR158, PR161, 159, 160

all resistor footprints in this area all changed to 0402, except PR148
P/N need Terry update to meet footprint.
nicole 06/11

| | |
|---|-----------------|
|  PROJECT : CH3 Quanta Computer Inc. | |
| Size | Document Number |
| CPU CORE (SC452) | |
| Date: | Rev 1A |
| Tuesday, February 06, 2007 | Sheet 37 of 46 |



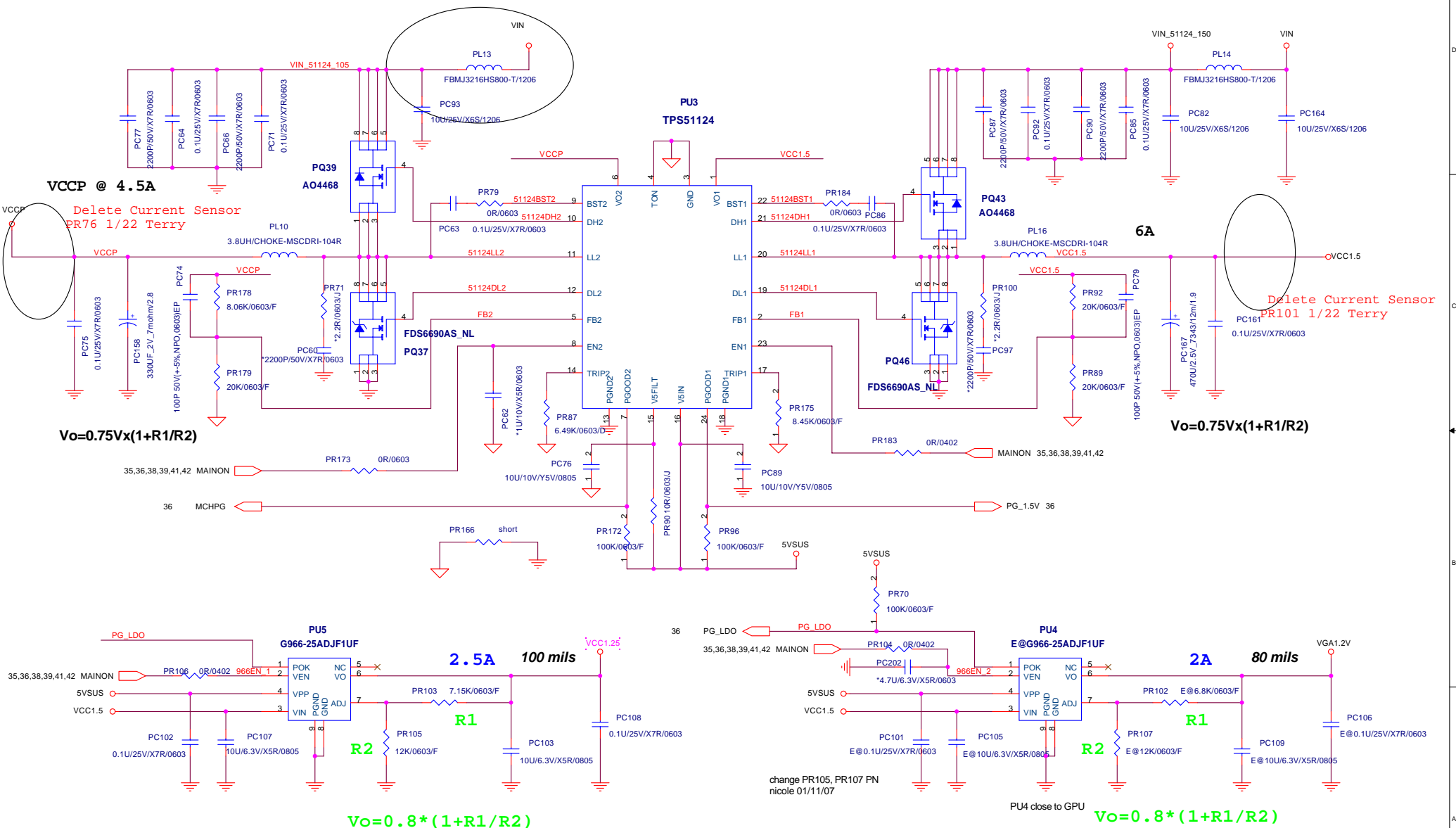


PROJECT :CH3
Quanta Computer Inc.

| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | GMCH (MAX8776) | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 39 of 46 |

hexamf@hotmail.com

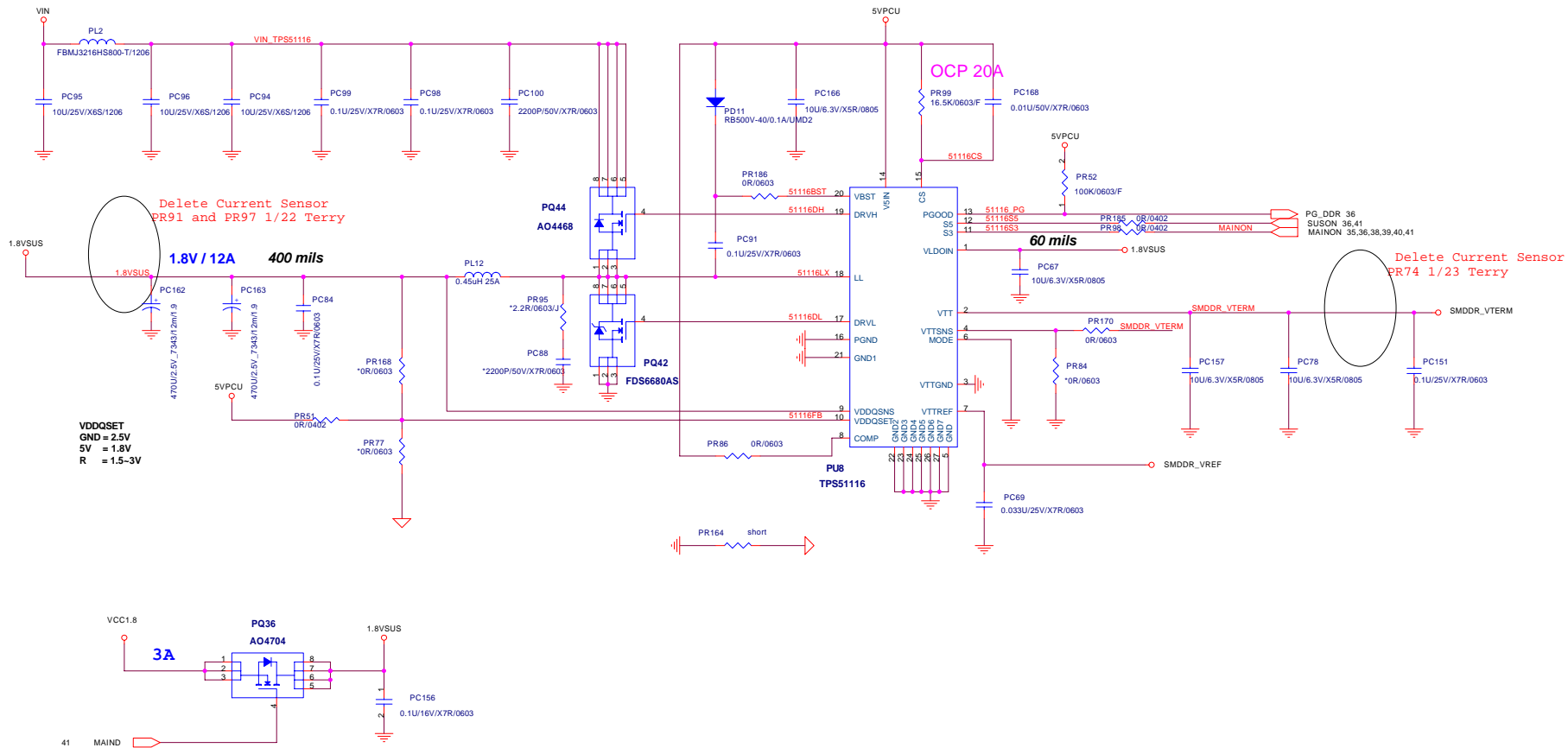
VCCP&VCC1.5V&VCC1.25&VGA1.2



PROJECT : CH3
Quanta Computer Inc.

| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | VCCP(1.05V)VCC1.5 | 1A |
| Date: | Tuesday, February 06, 2007 | Sheet 40 of 46 |

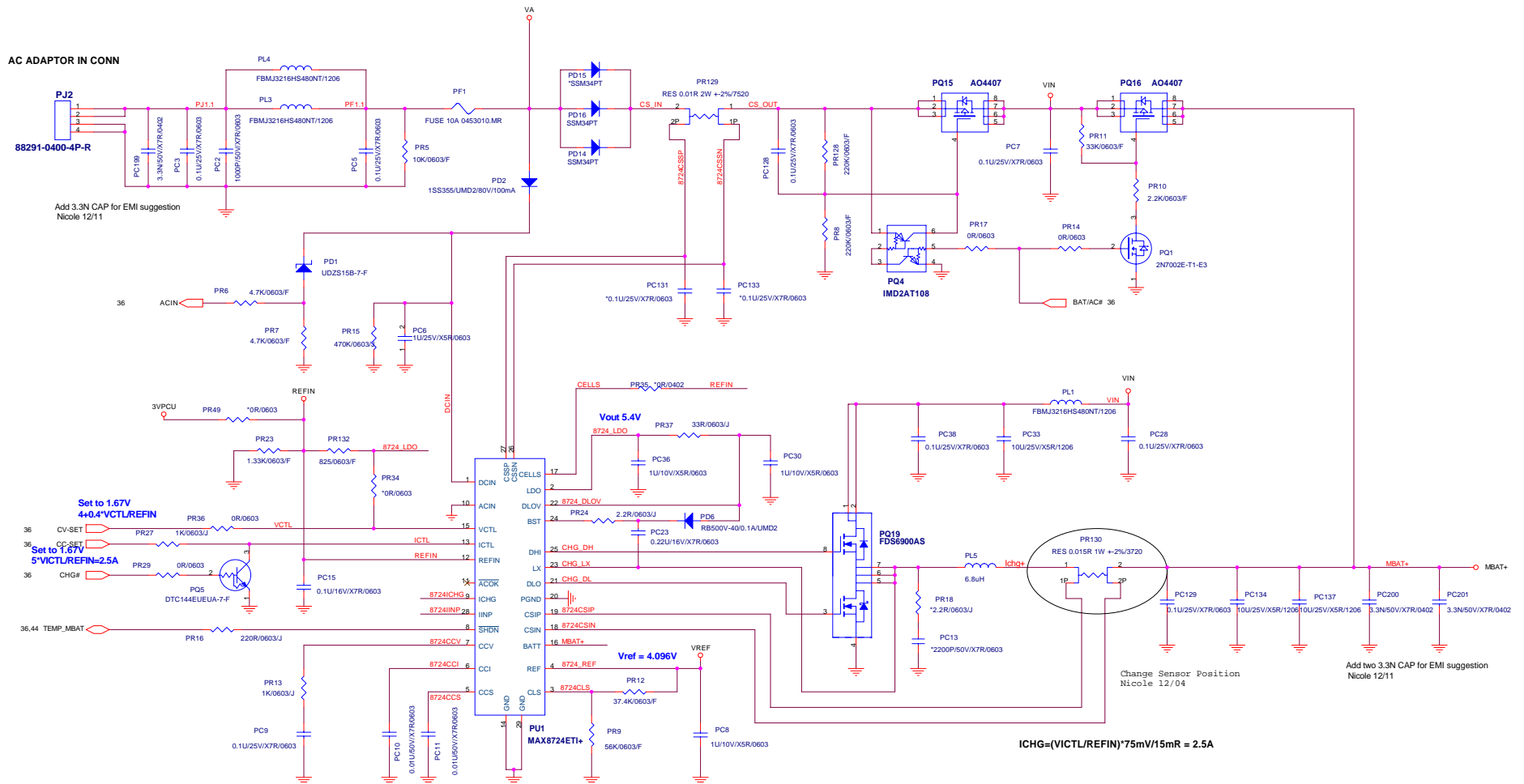
1.8VSUS & VCC1.8 & SMDDR_VTERM



AC ADAPTOR IN CONN

88291-0400-4P-R

Add 3.3N CAP for EMI suggestion
Nicole 12/11



Set to 1.67V
4*0.4*VCTL/REFIN

Set to 1.67V
5*VCTL/REFIN=2.5A

$$I_INPUT = [56 / (40.2 + 56)] * 75mV / 10mR = 3.966A \text{ (85W)}$$

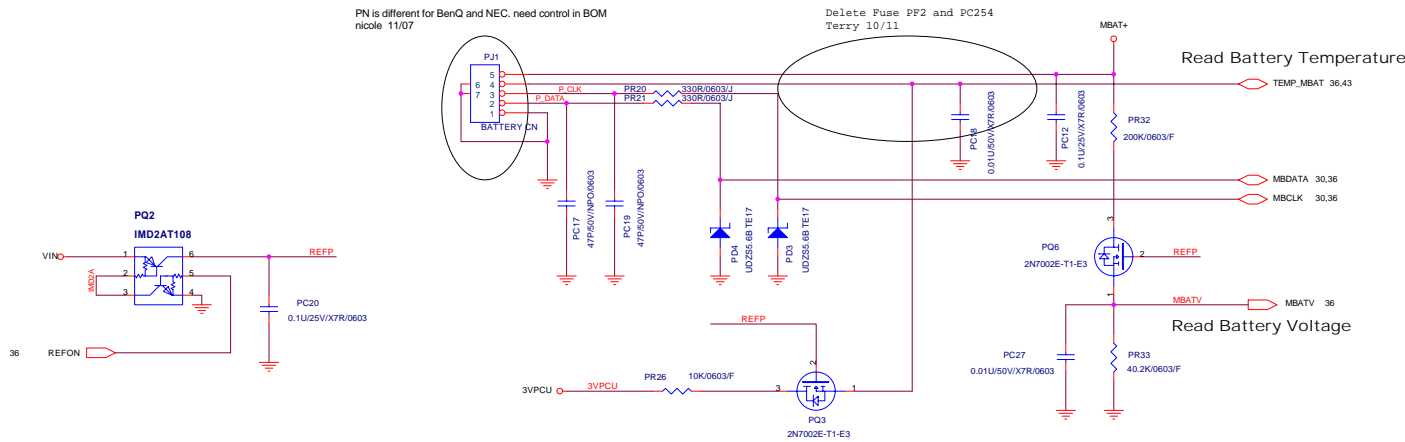
$$ICHG = (VCTL/REFIN) * 75mV / 15mR = 2.5A$$



| BATT-TYPE | |
|-------------|-------------|
| High | Low |
| Li-Ion 4S2P | Li-Ion 3S2P |
| Li-Ion 4S1P | Li-Ion 3S1P |
| Ni-MH 8S1P | |

Battery Connector

Battery Connector



PN is different for BenQ and NEC. need control in BOM
nicole 11/07

Delete Fuse PF2 and PC254
Terry 10/11

Read Battery Temperature

Read Battery Voltage

TEMP_MBAT voltage :

| | System Off | System On |
|-----------------|------------|-----------|
| Battery | 0V | 1.6V |
| Adapter | 3.3V | 3.3V |
| Battery+Adapter | 1.6V | 1.6V |

MBATV voltage :

| | |
|-------------|--|
| Li-ion 4S*P | $16.8V * 40.2 / (200 + 40.2) = 2.812V$ $12.0V * 40.2 / (200 + 40.2) = 2.008V$ |
| Ni-MH 8S1P | $8.0V * 40.2 / (200 + 40.2) = 1.34V$ |

CH3 B stage change list

1. P9. Del R117,R217,R233, R496, R485 and R486, update the relative net name. 12/01
2. P13. Update SDRAM SMbus clock and data net name 12/01
3. P17. Update the HW VRAM strap setting 12/01
4. P28. Del H27 12/01
5. P30. Del R398 12/01
6. P34. Change the capacities of C601 and C604 from 1u to 4.7u for Realtek AE suggestion 12/01
7. P34. Add digital MIC array 12/01
8. P35. Add R629, R630, R631 and R632, Change C838, C845 from 1u to 4.7u, C616, C611 from 1u to 2.2u . 12/01
9. P34. Add R635 and R636 in HDA_SDIN signal 12/05
10. P25. Del C6 and C13 for EDID CLK and DATA issue 12/05
11. P29. Update CN8 signal sequence, cable need update 12/05
12. P34, 35. Del Q28, R620, R621, add R637, R638 and C894 12/06
13. P39. Change PC170 from 10u to 1u 12/06
14. P33. Update CN23 footprint, need new PN 12/06
15. P14. Change R230 footprint to 0402 12/07
16. P2. Change U19 PN from B version to D version. 12/01
17. P24, P36. Change quick button function definition 12/08
18. P25. Change CN13 footprint from SMT to DIP. 12/04
19. P41. Change PQ12, PQ13 net name 12/08
20. P39. Change PQ41to AO4408, PQ45 to AO4410 12/08
21. P38. Change PQ40 to AOL1414, PQ11, PQ38 to AO4456 12/08
22. P2.P42. Add C895, C896, PC199, PC200, PC201 3.3nF for EMI issue 12/11
23. Add C897 and PC202 for frequency adjust 12/11
24. P39. Change MAX8776 FB net from +VGFX_CORE to VGFX_CORE 12/11
25. P25. Add magnetic sense LID SW for NEC 12/11
26. P31. Change U44 footprint, need apply new PN 12/11
27. P28. Del R327,R329, R551 and R554 for they have internal pull-up, del R532 and R556 for wrong connection 12/12
28. P16, P25. Add B channel LVDS signals for EXTERNAL SKU 12/12
29. P24. Change R427, R426, R428 from 150ohm to 330ohm, LED power change from VCC5, 5VPCU to VCC3 and 3VPCU 12/12
30. P25. Change LID SW footprint and PN for NEC 12/14
31. P36, P26. C770, C774 change from 10pF to 15pF, C808 from 22pF to 27pF. 12/14
32. P30. Change BT connector for NEC and BenQ share 12/14
33. P9. Del R170, R161, add R642 and change net +VCCA_MPLL_L 12/18

CH3 C stage change list

1. P25. Change SW pin definition for not coincident with layout library 01/05/07
2. P17. Update GPU PCI device strapping for NB8P-SE 01/11/07
3. P35. Change C611, C616 PN 01/11/07
4. P36. Change U10 PN 01/11/07
5. P40. Change PR105, PR107 PN 01/11/07
6. Delete CPU_Vcore Current Sensor:PR158, PR159, PR160, PR161 1/22
7. Delete Current Sensor PR188, PR76, PR101,PR119, PR112, PR91, PR97, PR74 1/22
8. P33. Change CN20 footprint 1/24
9. P24. Add R643, R644, R645 and R646 1/26
10. Delete CPUVcore 0 ohm resistor: PR142, PR144, PR43, PR147, PR149, PR150, PR153 02/01/07
11. Delete Max1993 0ohm resistors PR88, PR163, PR171, PR177 02/01/07
12. Delete SC452 reserved 0 ohm resistors: PR133, PR151 02/01/07
13. Delete Max8776 Reserved 0 ohm resistors: PR190, PR191, PR194, PR196, PR217, PR209, PC176 02/01/07
14. Delete TPS51124 Power Good Reserved 0 ohm resistor: PR80, PR94 02/01/07
15. Delete G966 Power Good Reserved 0 ohm resistor: PR110, PR108 02/01/07
16. Move PC93 behind PL13 02/01/07
17. Delete Max8734 Reserved 0 ohm resistors: PR123, PR221, PR121, PR224 02/01/07
18. Delete TPS51116 PC150, PR162, PR93, PR169, PR75 02/01/07
19. Del C740 and C693 02/05/07
20. Add R643, R644, R645 and R646 02/05/07
21. Add signal L2-ECO# 02/05/07
22. Change C732, C700, C842, C860 footprint 02/05/07
23. Change R10, R423-R428, R643-R646 from 330ohm to 150ohm 02/06/07
24. Del SW1 02/07/07
25. Stuff LP9--LP12 and change them footprint, unstuff 0ohm resistors 02/02/07

SLP_S3#(SUSB#):Control non-critical power plane when system into S3(Suspend to RAM)/S4(suspend to Disk)/S5(soft off).
SLP_S4#(SUSC#):1.Control non-critical power plane when system into S4(Suspend to Disk)/S5(soft off).Used to control DRAM power

